Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM+ICH9-M core logic

2008-01-01

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.		
Title	*Cover Sheet*	
Size: Custom	Document Number: *Montevina Blade UMA LA4101P*	Rev: 0.3
Date: Saturday, January 05, 2008	Sheet 1 of 46	

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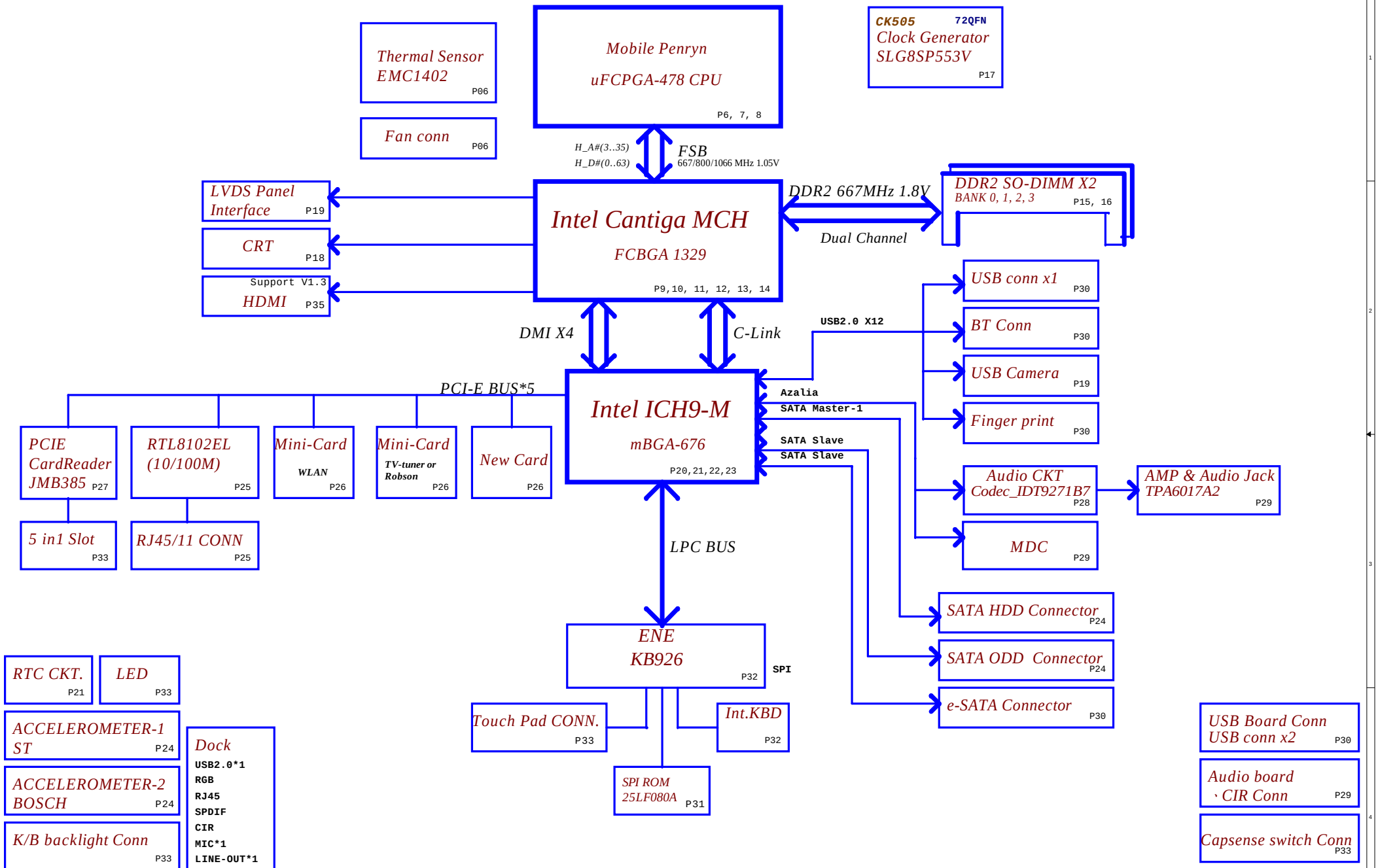
Montevina Consumer 14" UMA



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Title: **Block Diagram**

Size	Document Number	Rev
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Date: Saturday, January 05, 2008 Sheet 2 of 46

Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
Multi @ :	means just reserve for Multi Bay
NewC@ :	means just reserve for New card
DOCK@ :	means just reserve for Docking
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot

USB assignment:

USB-0	Right side
USB-1	Right side
USB-2	Left side(with ESATA)
USB-3	Dock
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

PCIe assignment:

PCIe-1	TV /WWAN/Robeson
PCIe-2	X
PCIe-3	WLAN
PCIe-4	GLAN (Realtek)
PCIe-5	Card reader
PCIe-6	New Card

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X	V	V
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

43154432L01 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/Multi@/2MiniC@
43154432L02 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/2MiniC@
43154432L03 : Main@/DEBUG@/DOCK@/NewC@/FP@/2MiniC@
43154432L04 : OPP@/DEBUG@
43154432L05 : OPP@/DEBUG@

43154432L01 : UMA GM PA FF (SI-1)
43154432L02 : UMA GM PR FF (SI-1)
43154432L03 : UMA GL PR FF-
43154432L04 : UMA GM OPP (SI-1)
43154432L05 : UMA GL OPP

Cantiga GM45 B0(QR32) : SA00001P930
ICH9M A2 ES2 Base : SA00002AN10

DA600007100 --->Main
DAZ03V00100 --->OPP

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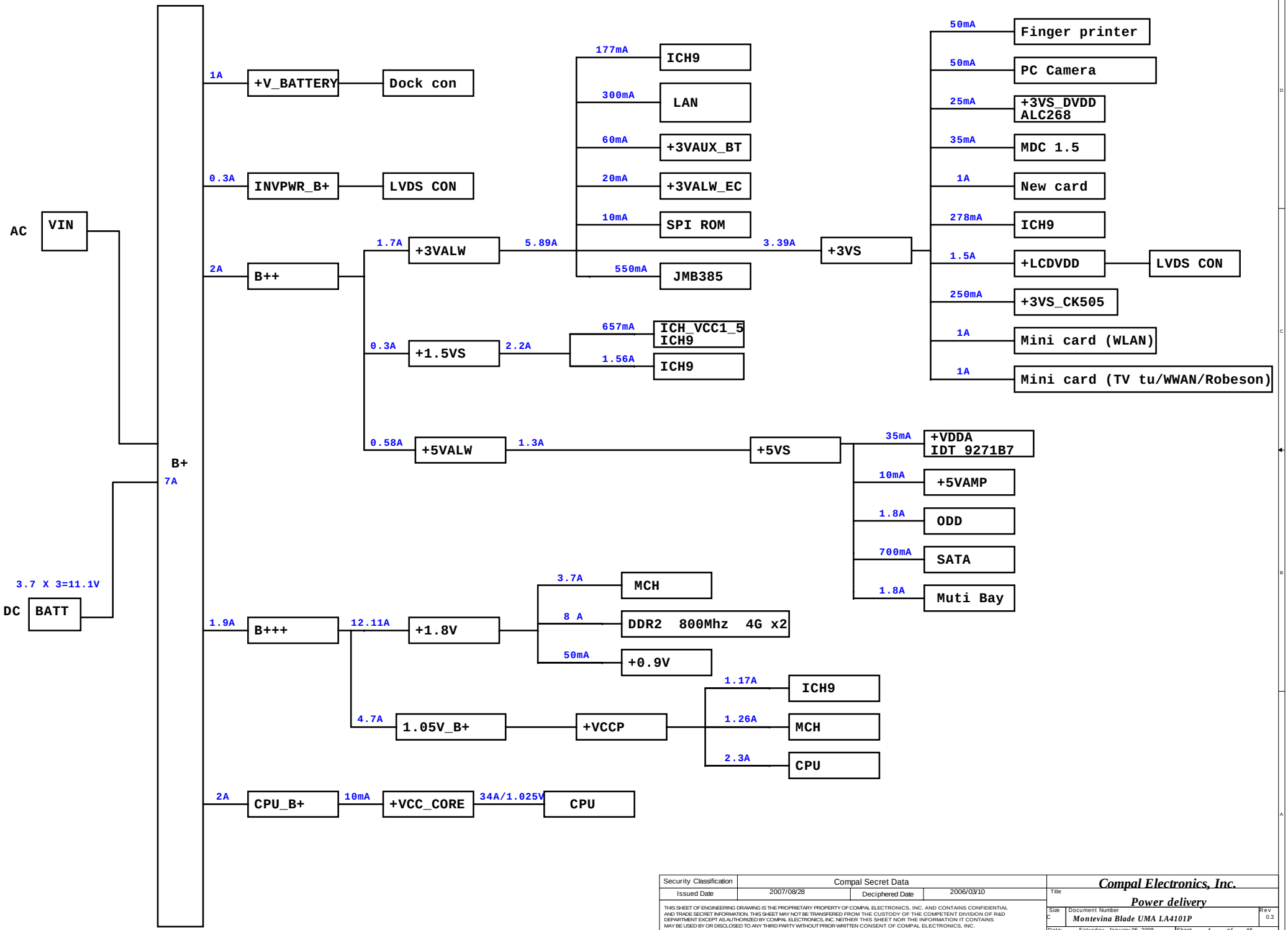
Title: Notes List

Size: Custom | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 3 of 46



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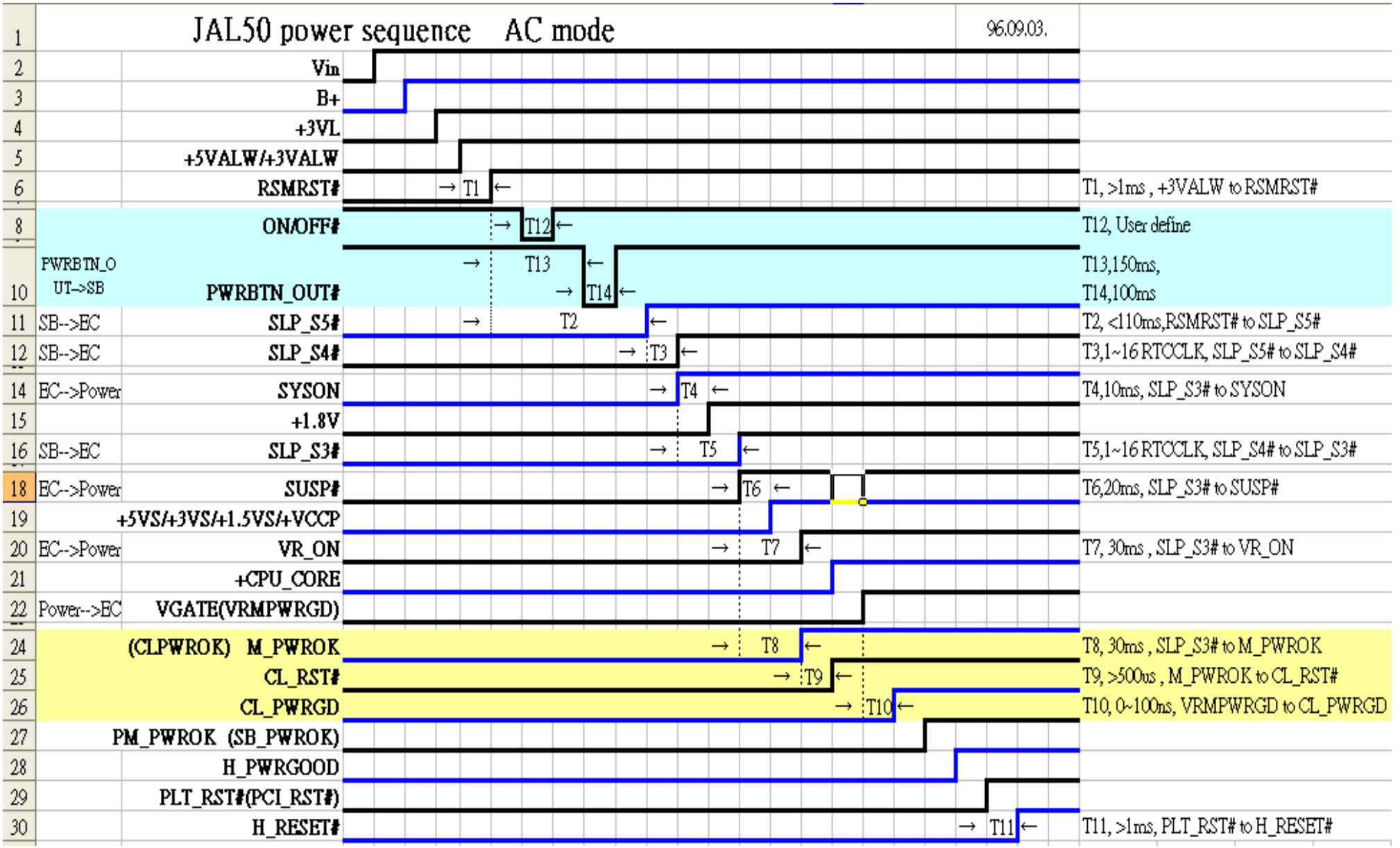
Title: Power delivery

Size	Document Number	Rev
C	Montevina Blade UMA LA4101P	0.3

Date: Saturday, January 05, 2008 Sheet 4 of 46



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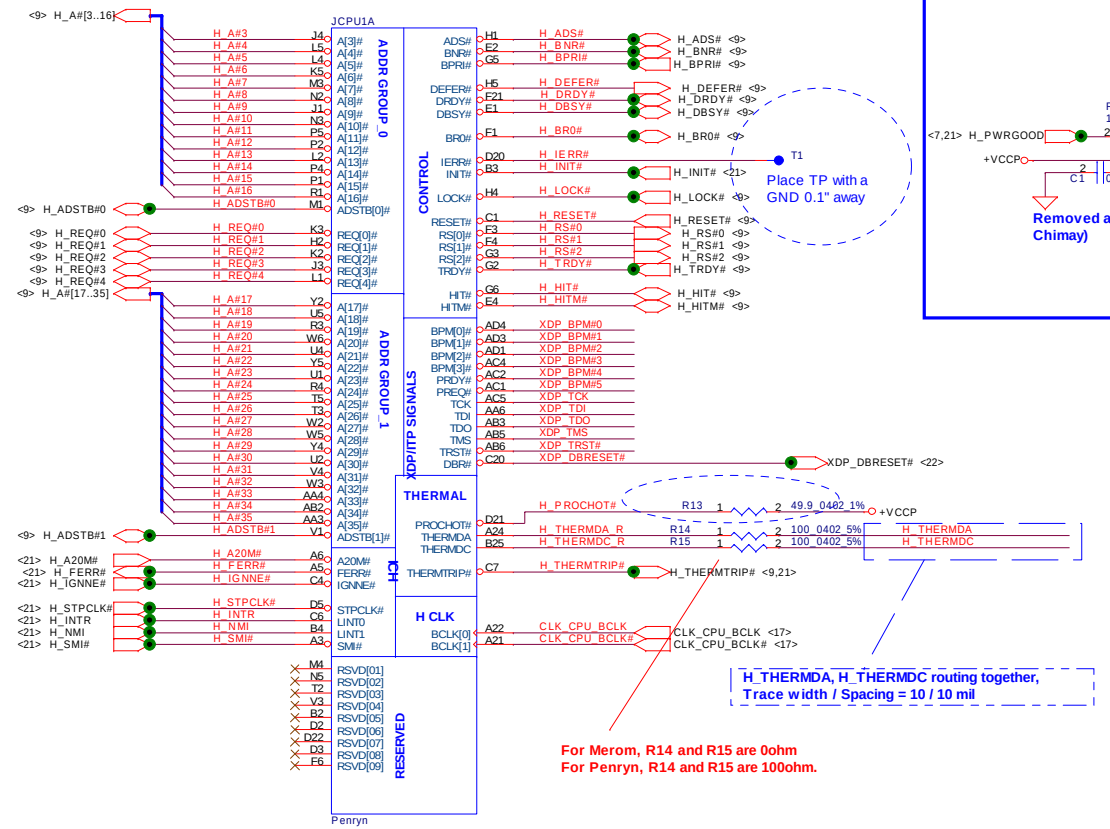
Issued Date	2007/08/28	Deciphered Date	2006/03/10

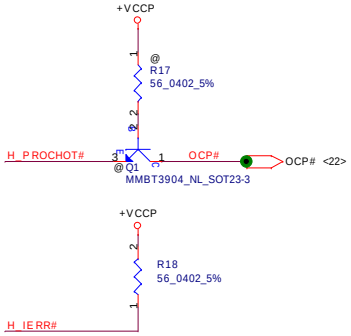
Compal Electronics, Inc.

Title: **Power sequence**

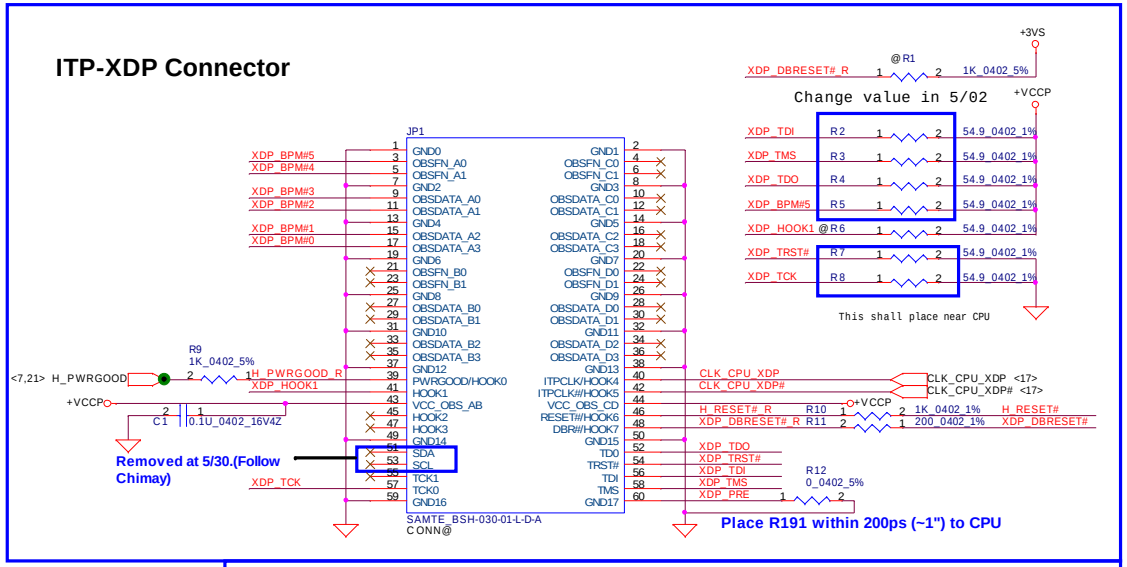
Size	Document Number	Rev
Custom	*Montevina Blade UMA LA4101P*	0.3

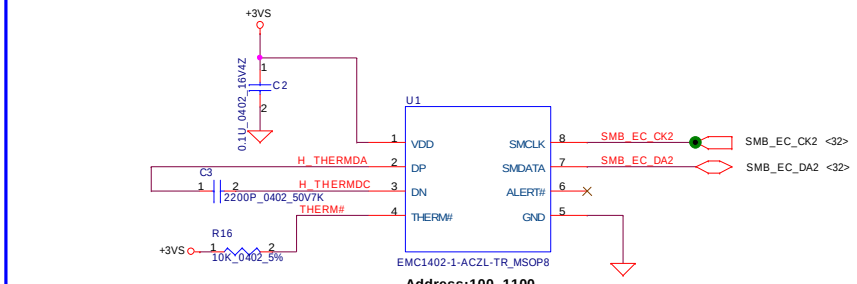
Date: Saturday, January 05, 2008 Sheet 5 of 46



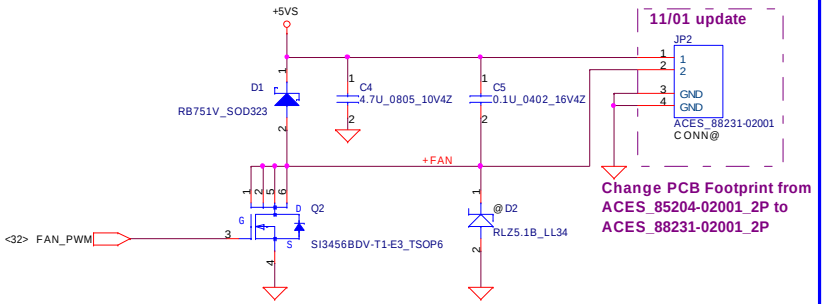


ITP-XDP Connector





PWM Fan Control circuit



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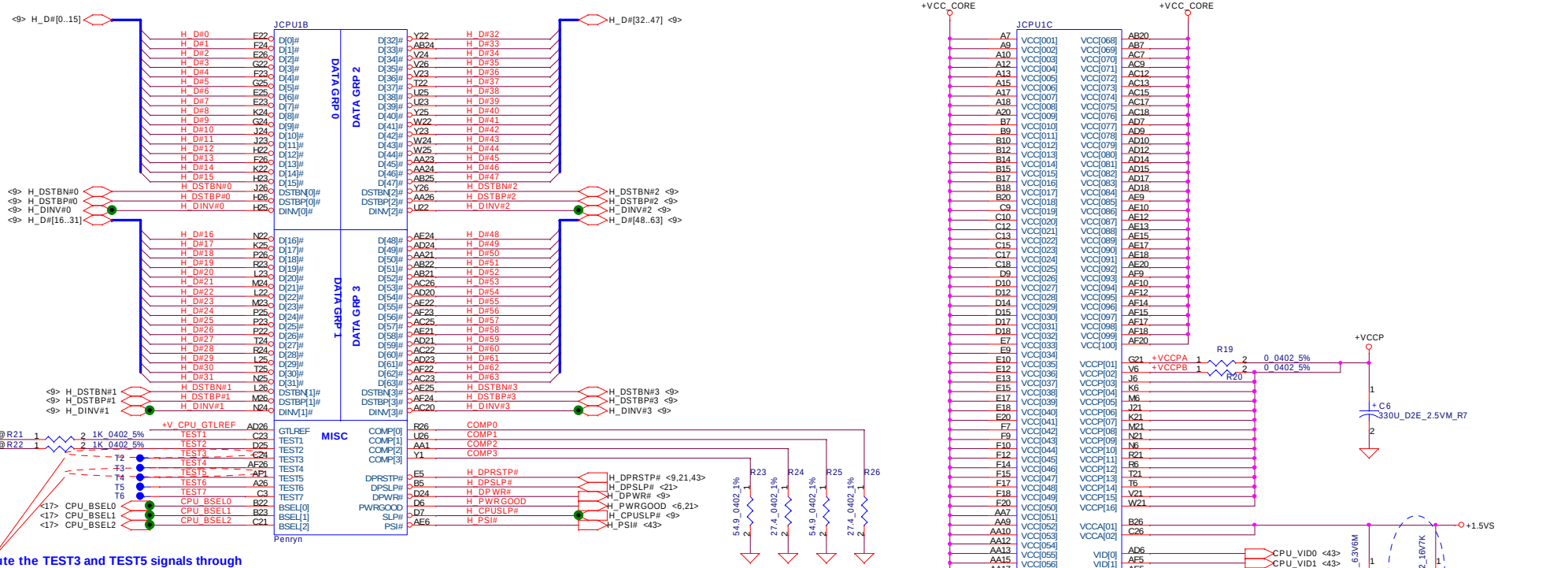
Compal Electronics, Inc.

Title: **Penryn(1/3)-AGTL+/ITP-XDP**

Size: Custom | Document Number: **Montevina Blade UMA LA4101P** | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 6 of 46



* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Close to CPU pin AD26 within 500mils.

Length match within 25 mils.
The trace width/space/other is 20/7/25.

Close to CPU pin within 500mils.

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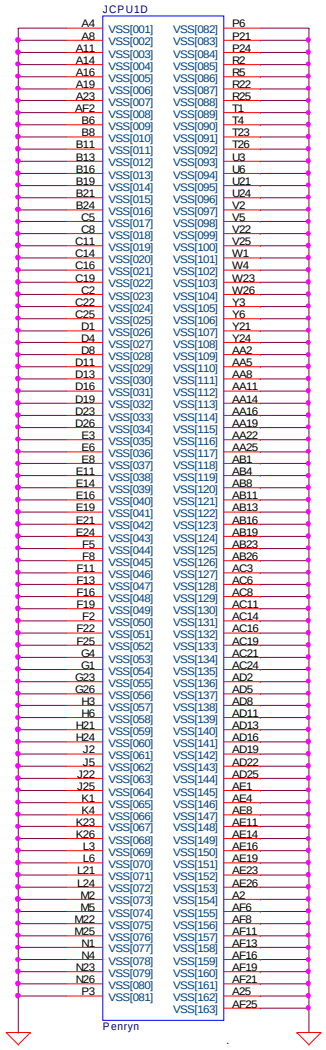
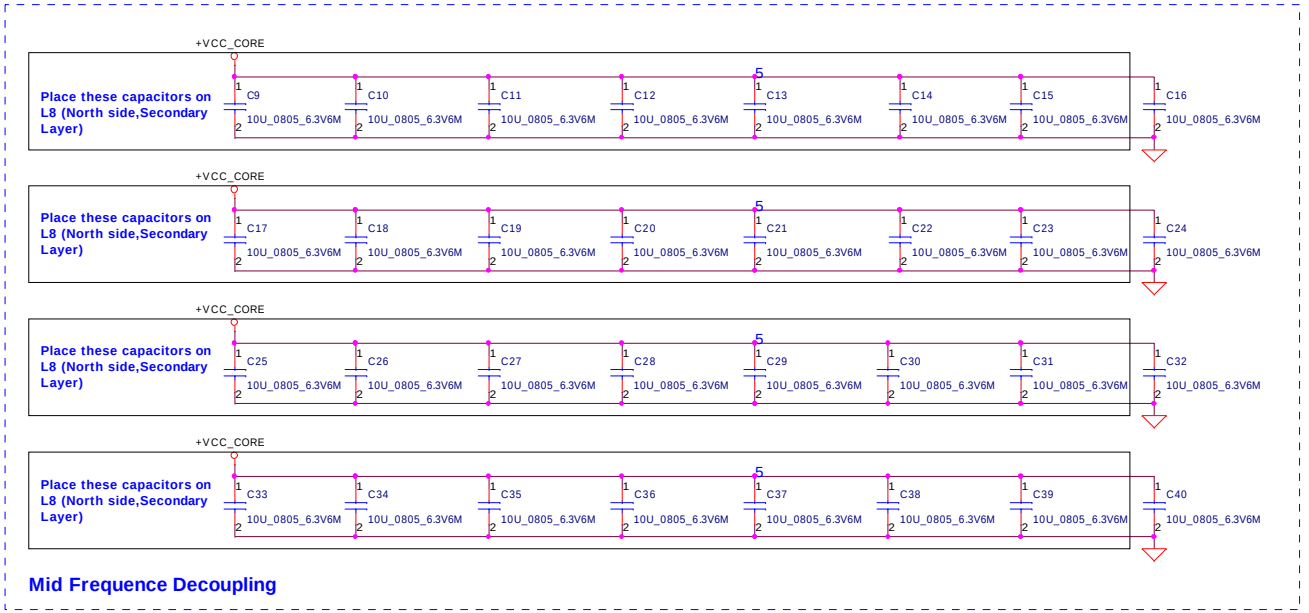
Compal Electronics, Inc.

Title: Penryn(2/3)-AGTL+/ITP-XDP

Size: Custom | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

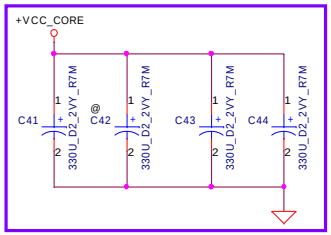
Date: Saturday, January 05, 2008 | Sheet 7 of 46



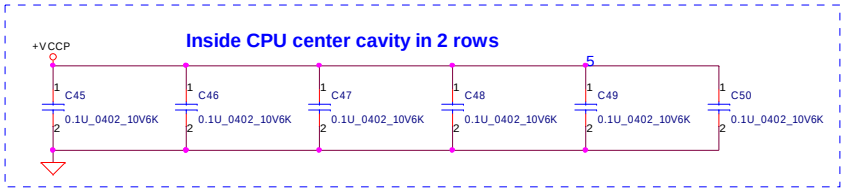


Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF



11/21 Change ESR=7m ohm



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Title: Penryn(3/3)-AGTL+/ITP-XDP		
Size: Custom	Document Number: Montevina Blade UMA LA4101P	Rev: 0.3
Date: Saturday, January 05, 2008	Sheet 8 of 46	

Layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG trace width and spacing is 10/20

within 100 mils from NB

Near B3 pin

Layout Note: V_DDR_MCH_REF trace width and spacing is 20/20.

+V_DDR_MCH_REF generated by DC-DC

0621 add CLK and DAT for DVI

*R44*Follow Intel feedback

0830 Add pull-up and pull-down resistor.

Follow Design Guide For Cantiga: 80.6ohm

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Compal Electronics, Inc.

Title: **Cantiga(1/6)-AGTL/DMI/DDR**

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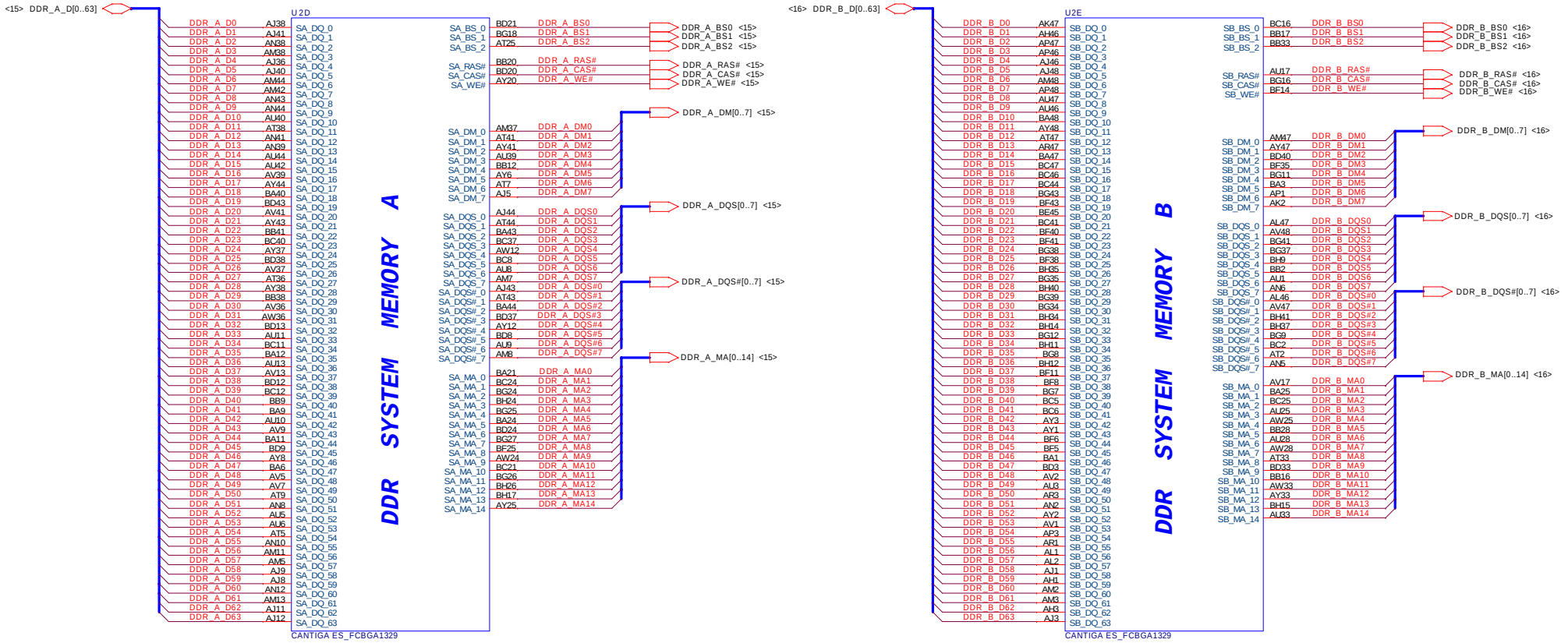
Date: Saturday, January 05, 2008 | Sheet 9 of 46



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Compal Electronics, Inc.

Title: **Cantiga(2/6)-DDR2 A/B CH**

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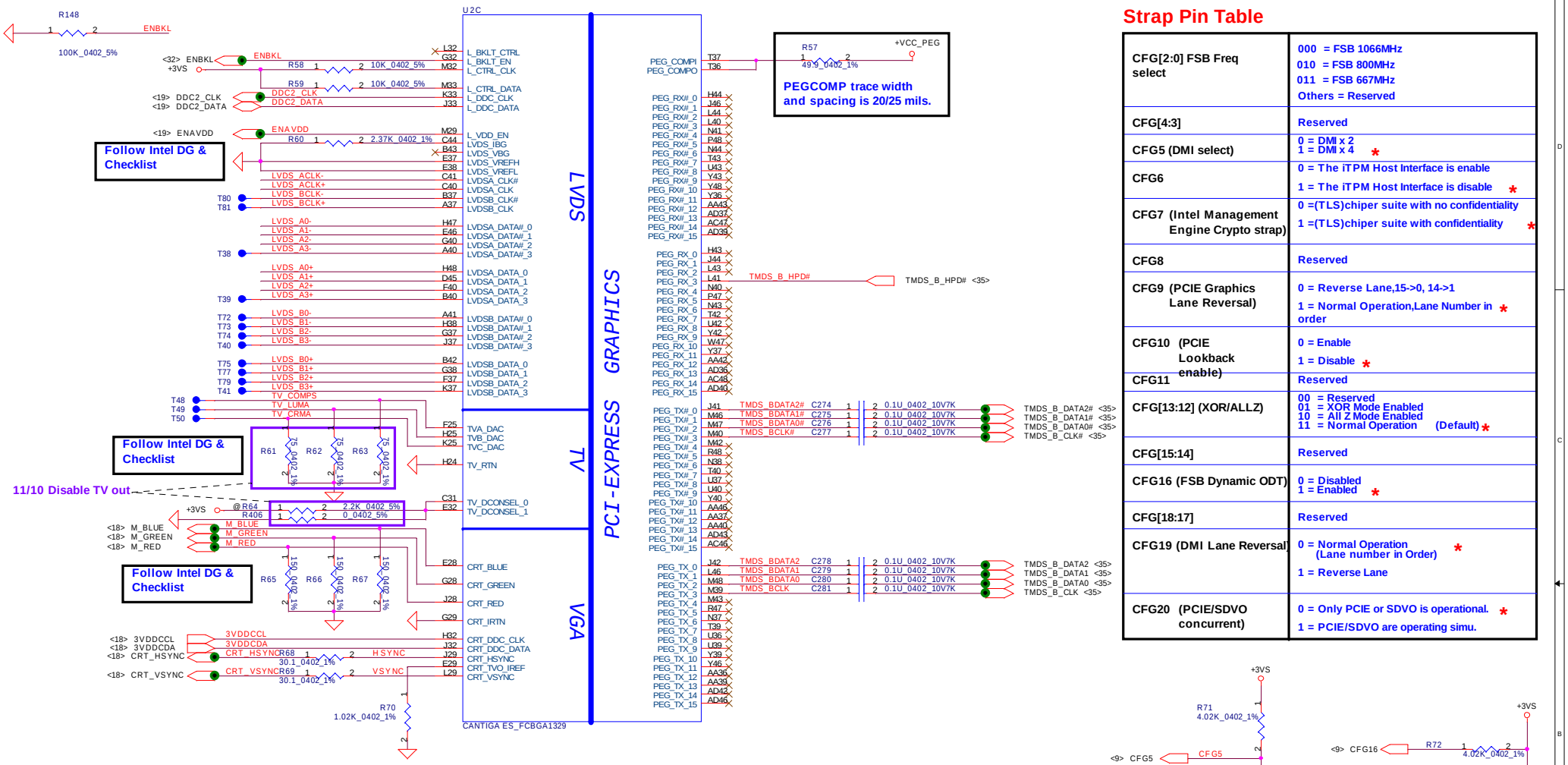
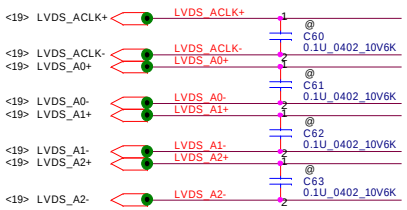
Date: Saturday, January 05, 2008 | Sheet 10 of 46



Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

Solve 3G WWAN issue



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Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Cantiga(3/6)-VGA/LVDS/TV**

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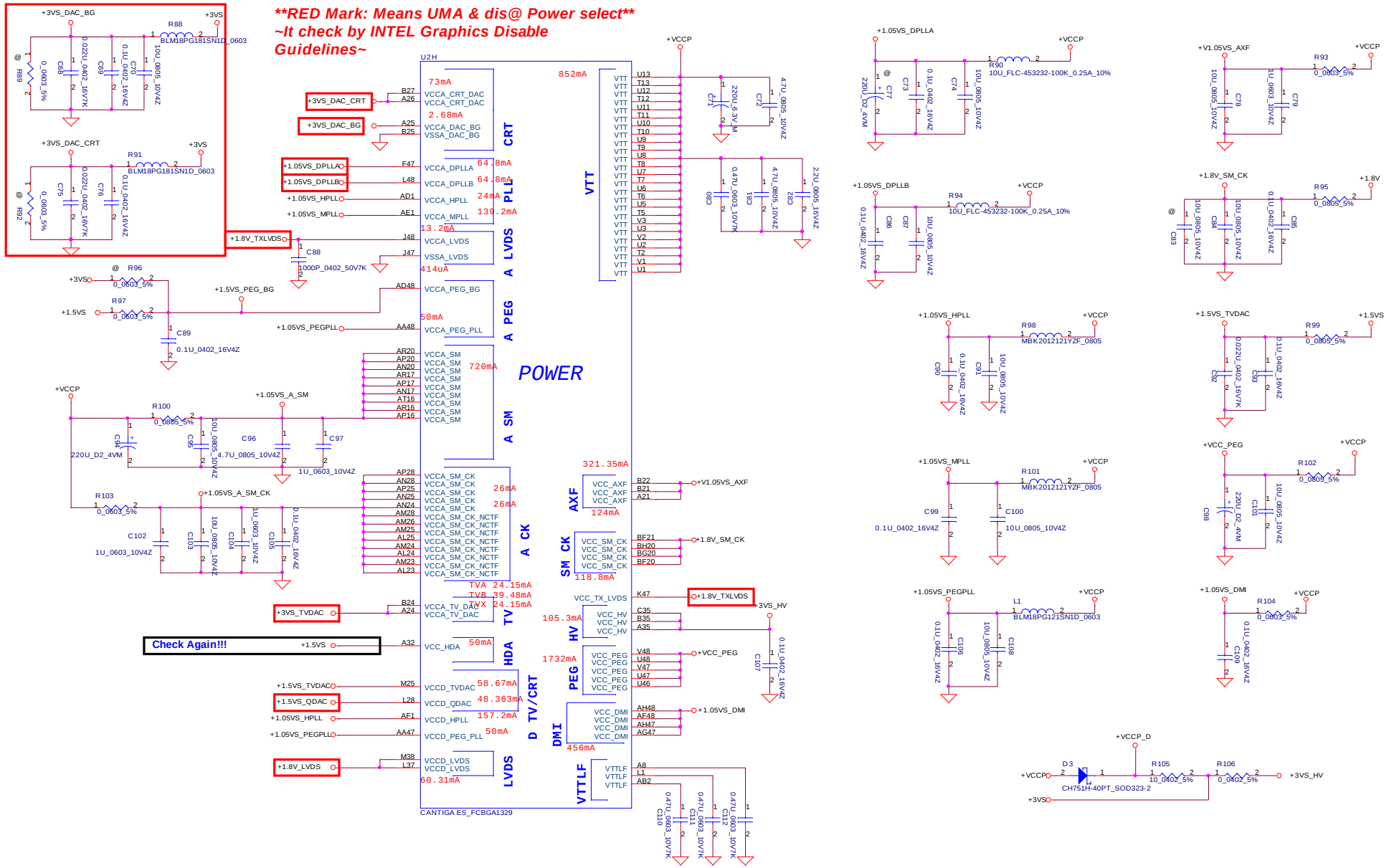
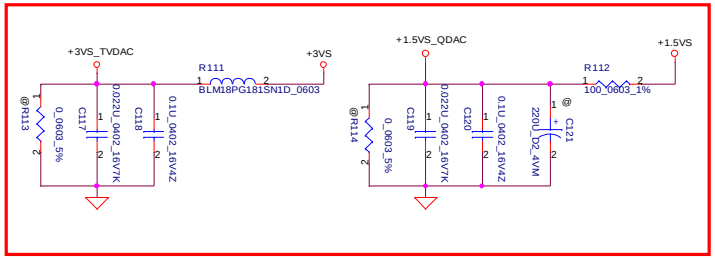
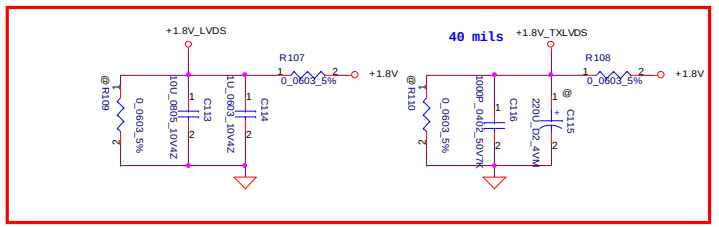
Date: Saturday, January 05, 2008 | Sheet 11 of 46

****RED Mark: Means UMA & dis@ Power select****
~It check by INTEL Graphics Disable Guidelines~







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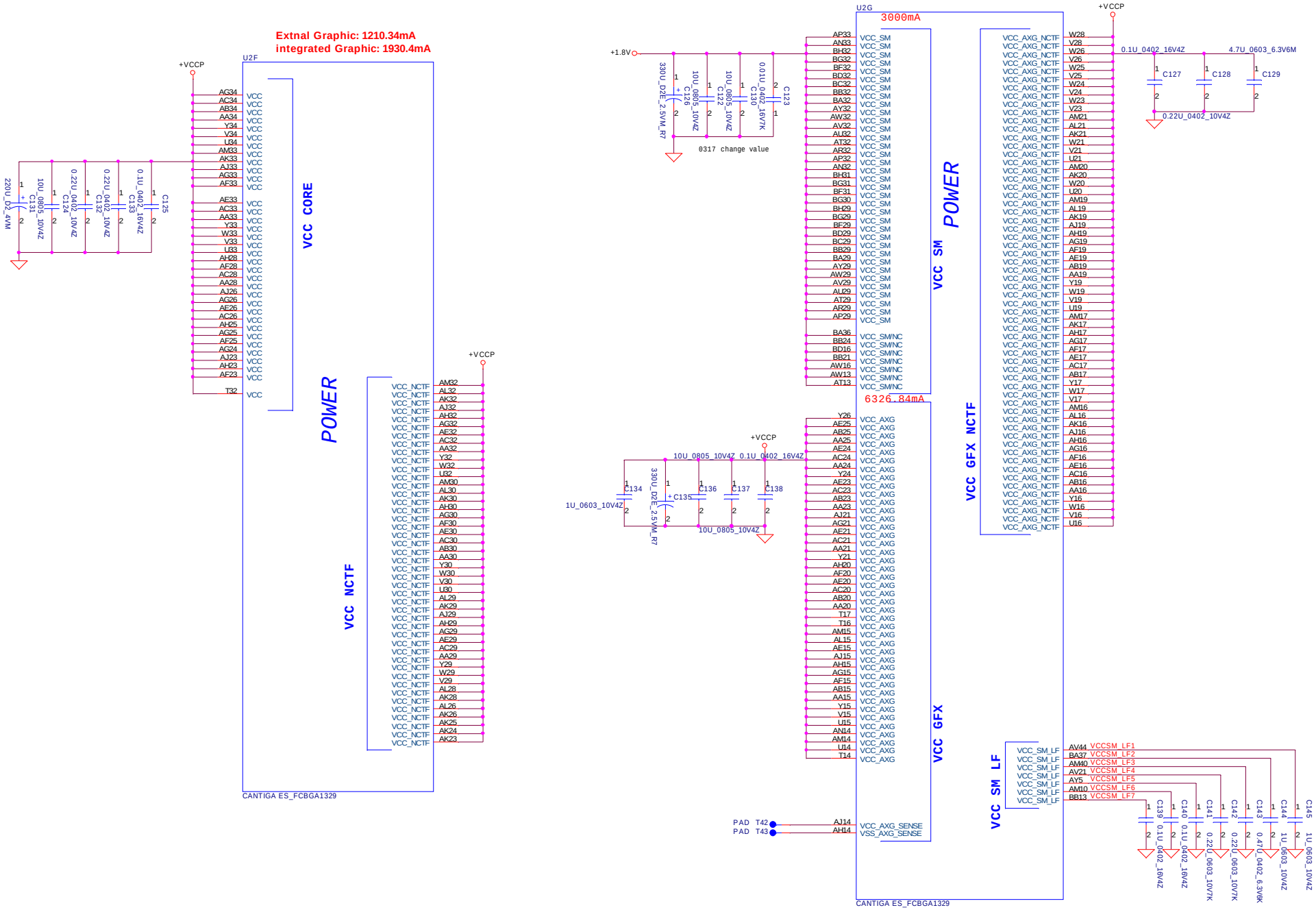
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Cantiga(4/6)-PWR**

Size: Custom | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 12 of 46



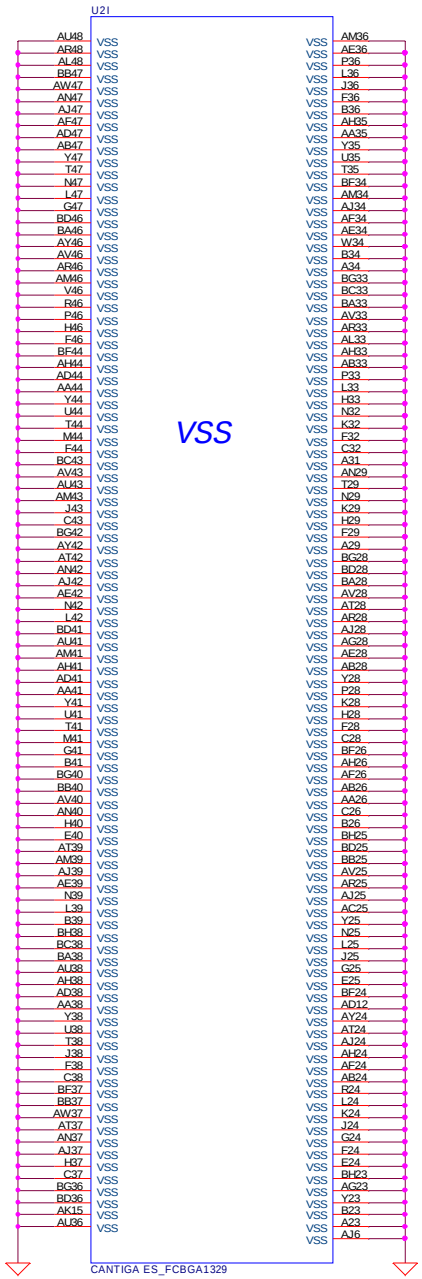
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

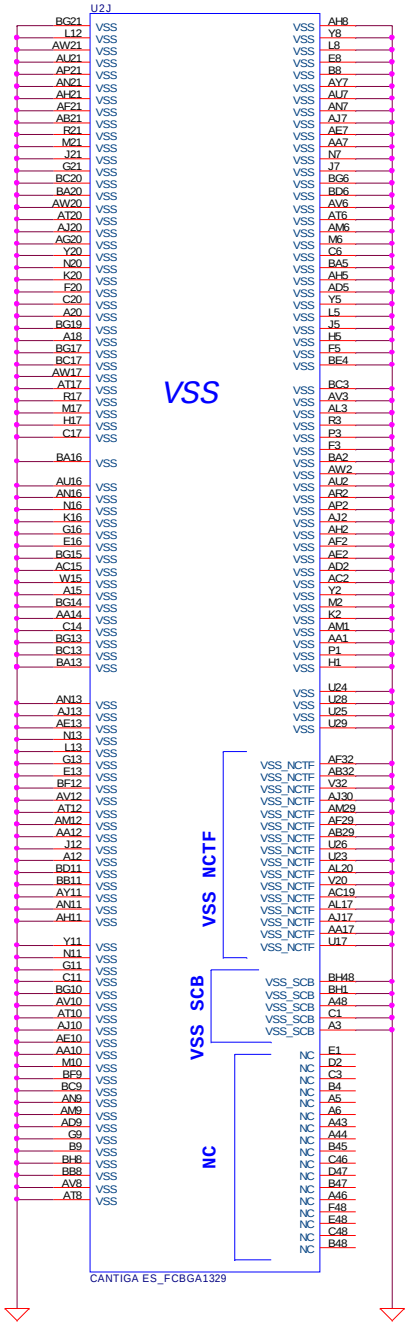
Compal Electronics, Inc.

Title: **Cantiga(5/6)-PWR/GND**

Size	Document Number	Rev
Custom	Montevina Blade UMA LA4101P	0.3

Date: Saturday, January 05, 2008 | Sheet 13 of 46





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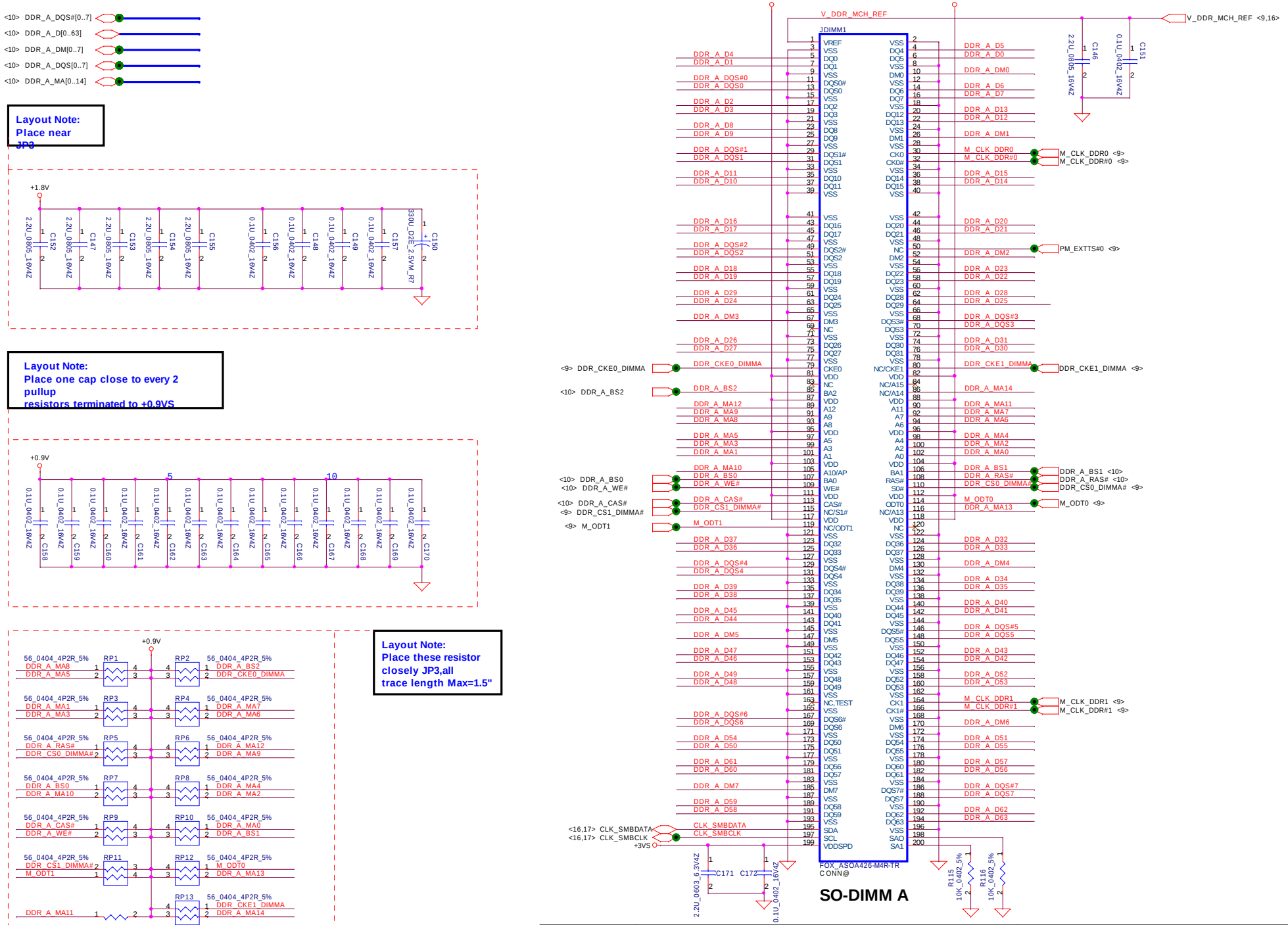
Compal Electronics, Inc.

Title: **Cantiga(6/6)-PWR/GND**

Size	Document Number	Rev
Custom	Montevina Blade UMA LA4101P	0.3

Date: Saturday, January 05, 2008 | Sheet 14 of 46



Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2006/03/10

Compal Electronics, Inc.

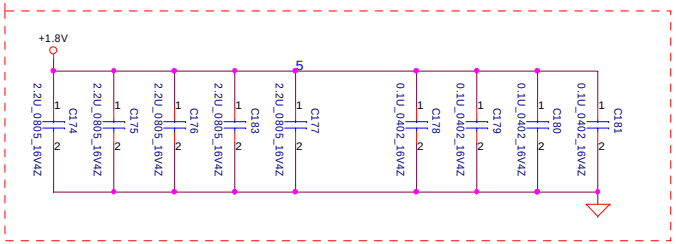
Title: **DDRII-SODIMM SLOT1**

Size	Document Number	Rev
Custom	Montevina Blade UMA LA4101P	0.3

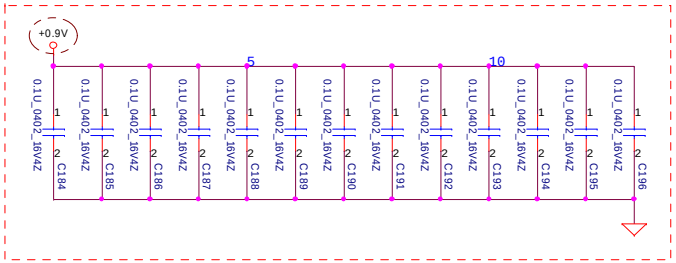
Date: Saturday, January 05, 2008 Sheet 15 of 46

<10> DDR_B_DQS#[0..7]
<10> DDR_B_D[0..63]
<10> DDR_B_DM[0..7]
<10> DDR_B_DQS[0..7]
<10> DDR_B_MA[0..14]

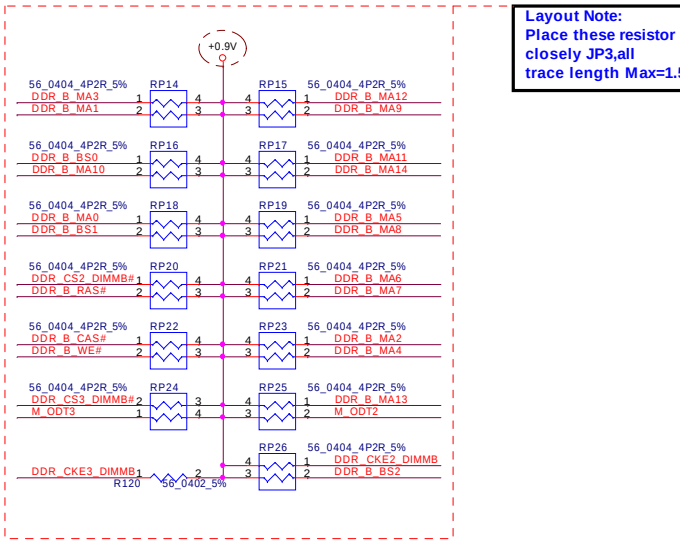
Layout Note:
Place near JP10

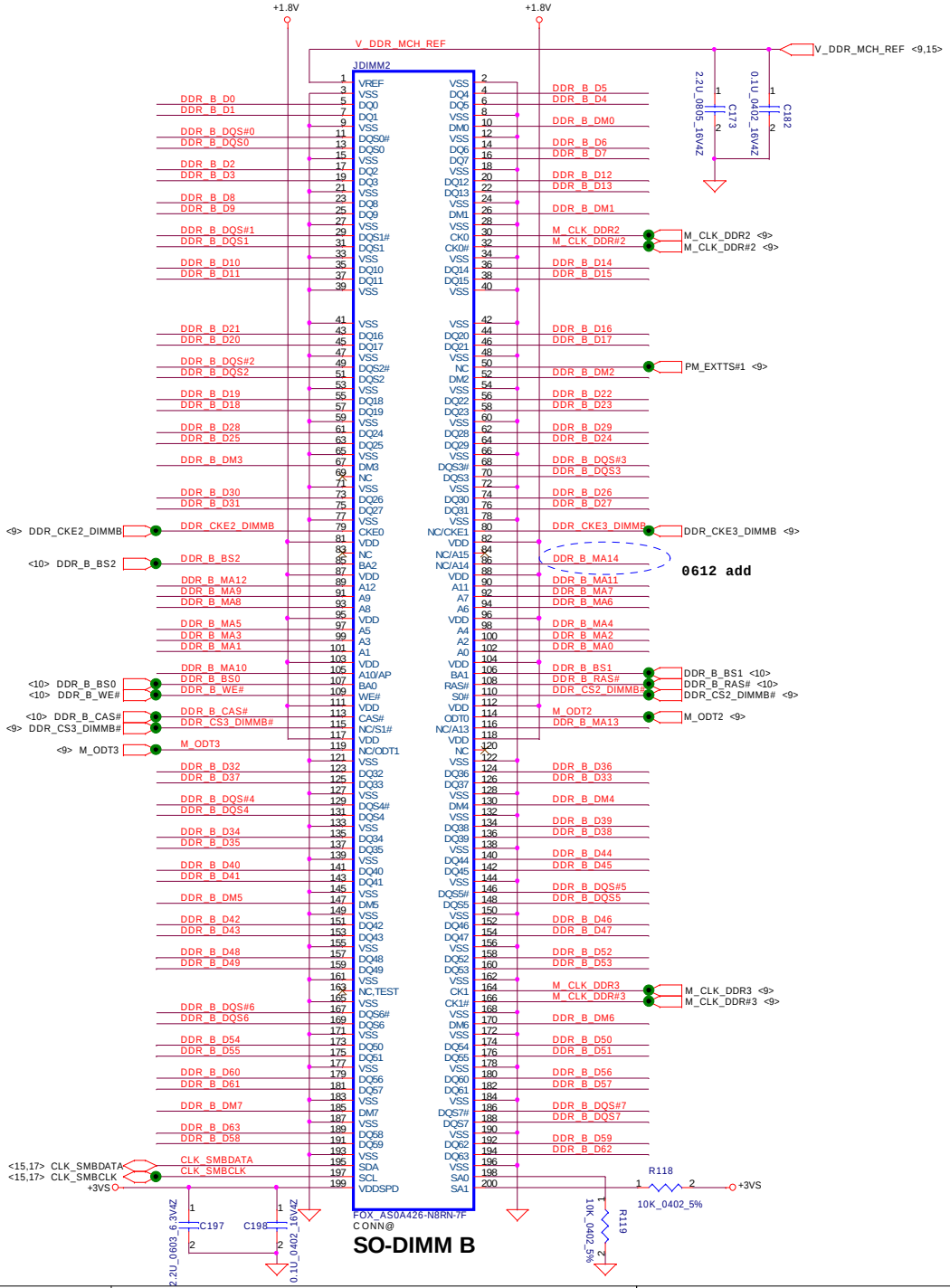


Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP3,all trace length Max=1.5"





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Compal Electronics, Inc.

Title: **DDRII-SODIMM SLOT2**

Size	Document Number	Rev
	Montevina Blade UMA LA4101P	0.3

Date: Saturday, January 05, 2008 | Sheet 16 of 46

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

Routing the trace at least 10mil

Place close to U51

Vendor suggests 22pF

Change 33M and 48M damping to 39M by EMI request

No Debug port anymore

ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)

<BOM Structure>

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

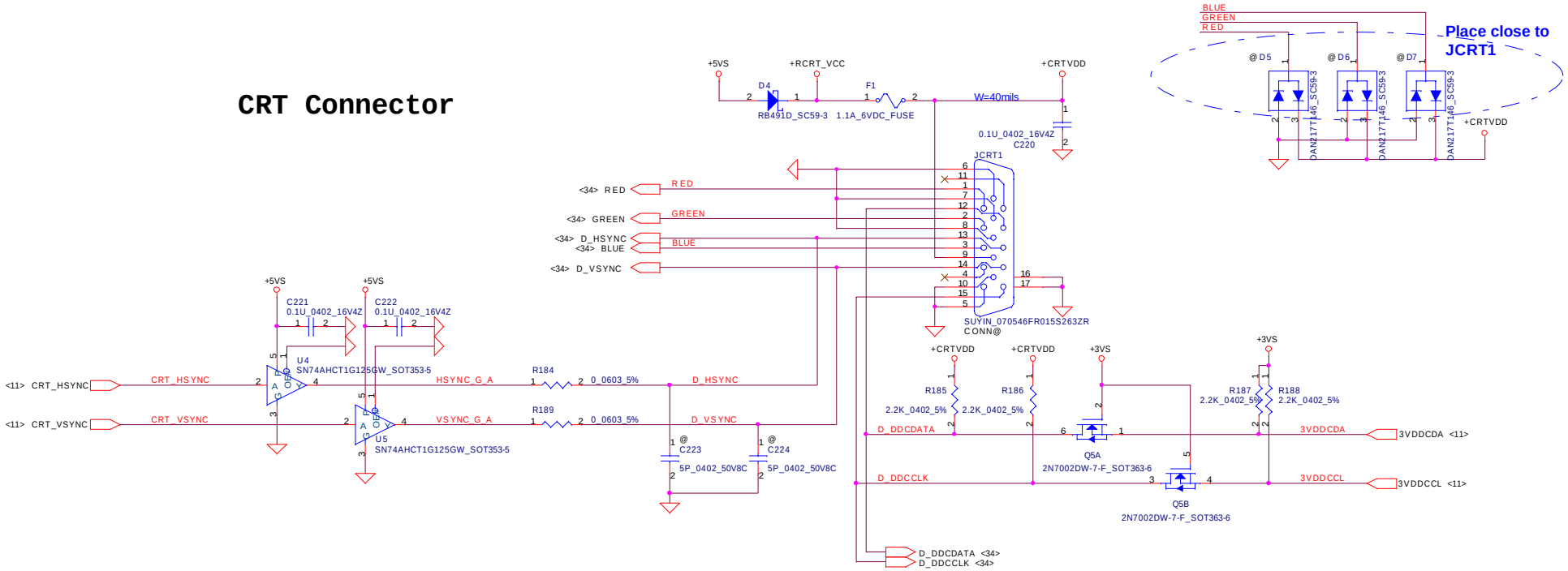
Compal Electronics, Inc.

Title: Clock Generator CK505

Size | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

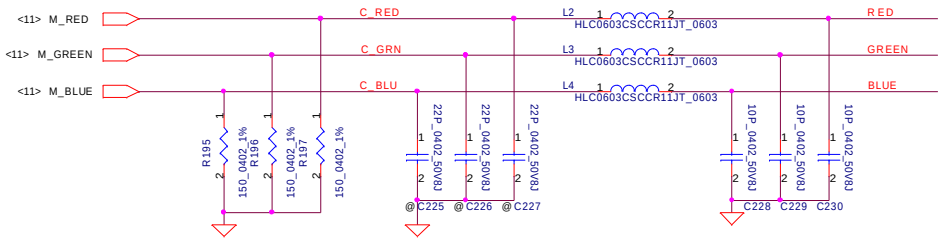
Date: Saturday, January 05, 2008 | Sheet 17 of 46

CRT Connector



CRT Termination/EMI Filter

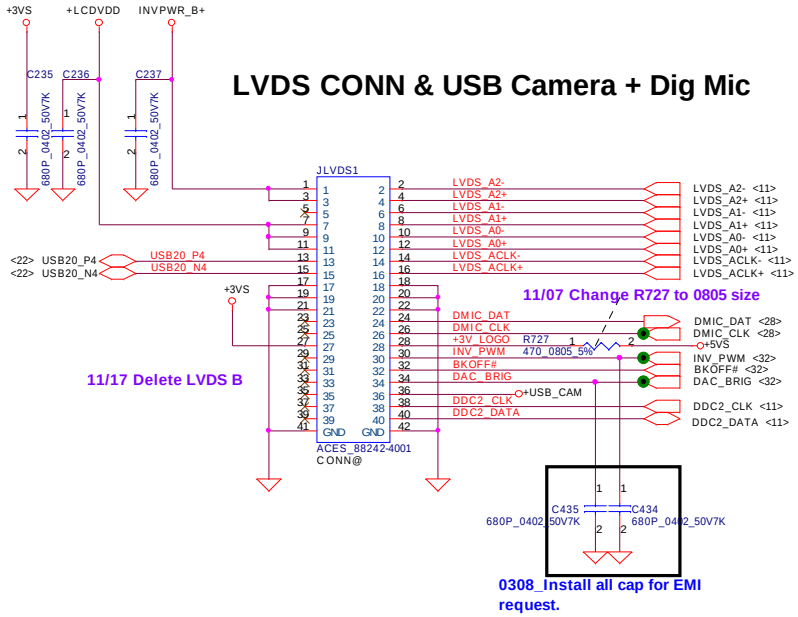
11/07 Change CRT lounting NB-->Docking-->CRT connector



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title	CRT Connector		
Size	Document Number	Montevina Blade UMA LA4101P	Rev 0.3
Date: Saturday, January 05, 2008	Sheet 18 of 46		

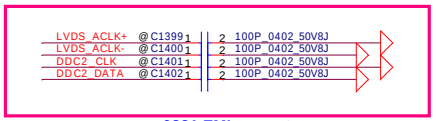
LVDS CONN & USB Camera + Dig Mic



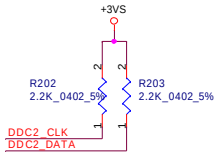
11/07 Change R727 to 0805 size

11/17 Delete LVDS B

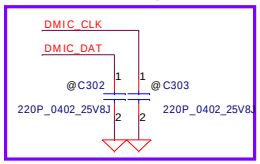
0308_Install all cap for EMI request.



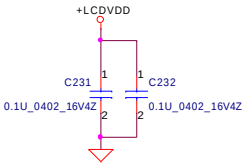
0831 EMI request

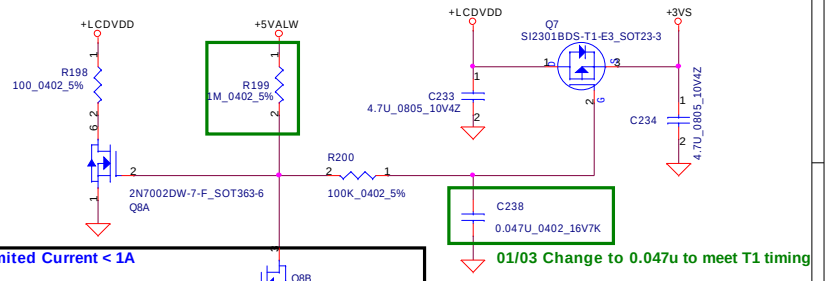


Must close JLVDS1pin 24、26

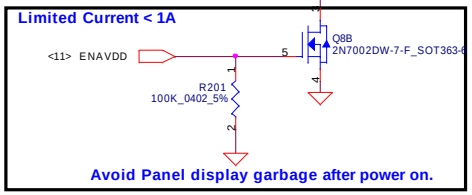


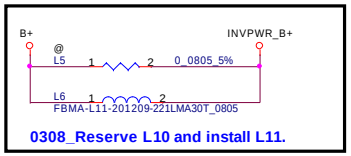
11/09 EMI reserver



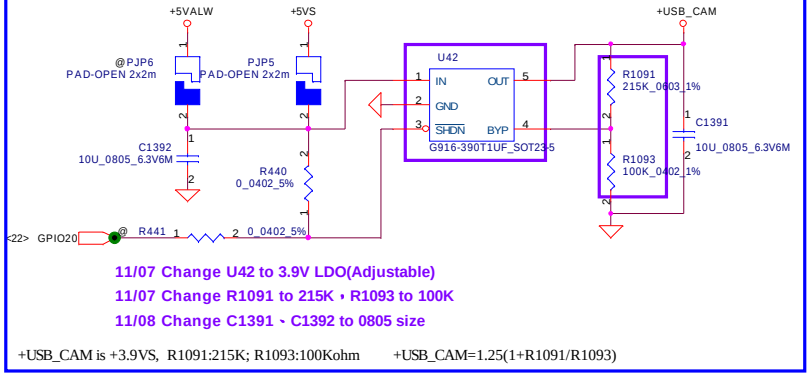


01/03 Change to 0.047u to meet T1 timing





USB Camera



11/07 Change U42 to 3.9V LDO(Adjustable)

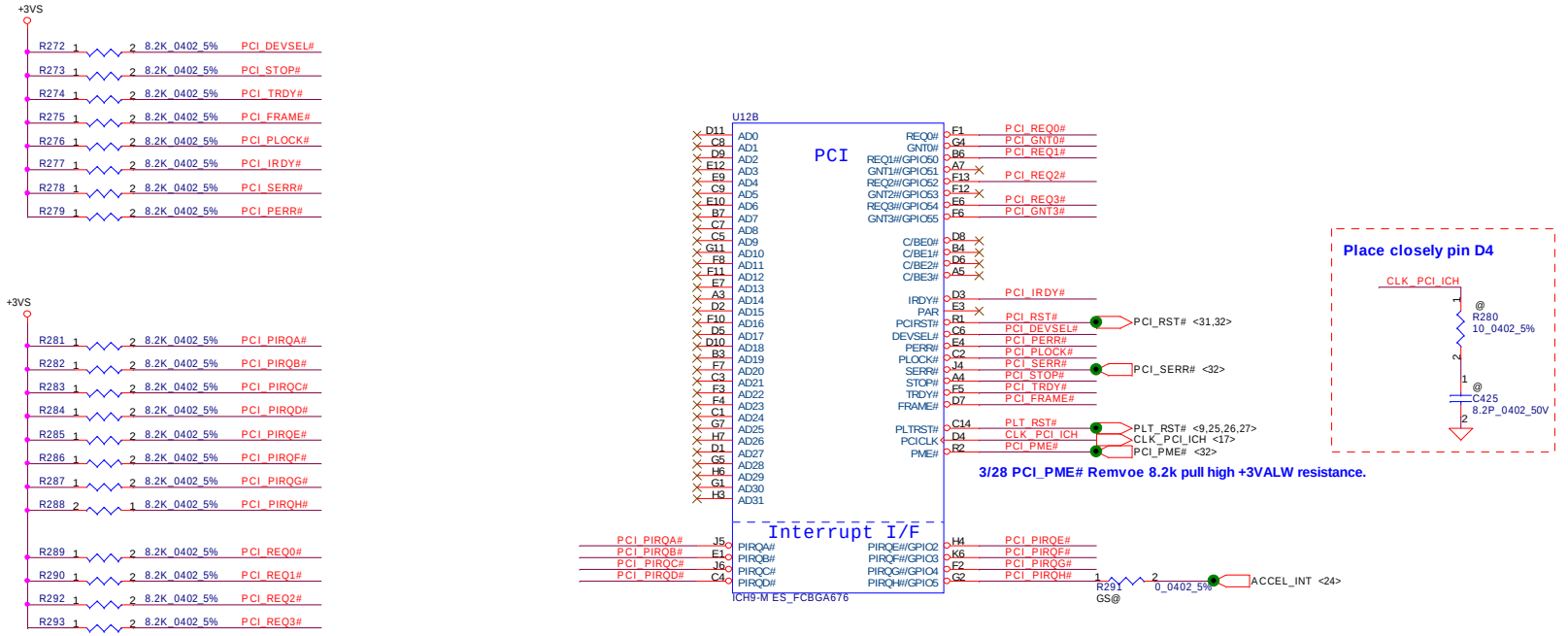
11/07 Change R1091 to 215K、R1093 to 100K

11/08 Change C1391、C1392 to 0805 size

+USB_CAM is +3.9VS, R1091:215K; R1093:100Kohm +USB_CAM=1.25(1+R1091/R1093)

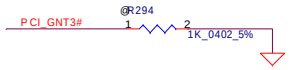
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.	
Title	LCD CONN.
Size	Document Number: Montevina Blade UMA LA4101P
Rev	0.3
Date: Saturday, January 05, 2008	Sheet 19 of 46



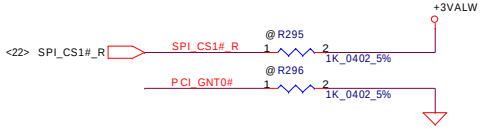
A16 swap override Strap

PCI_GNT3#	Low= A16 swap override Enble High= Default *



Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

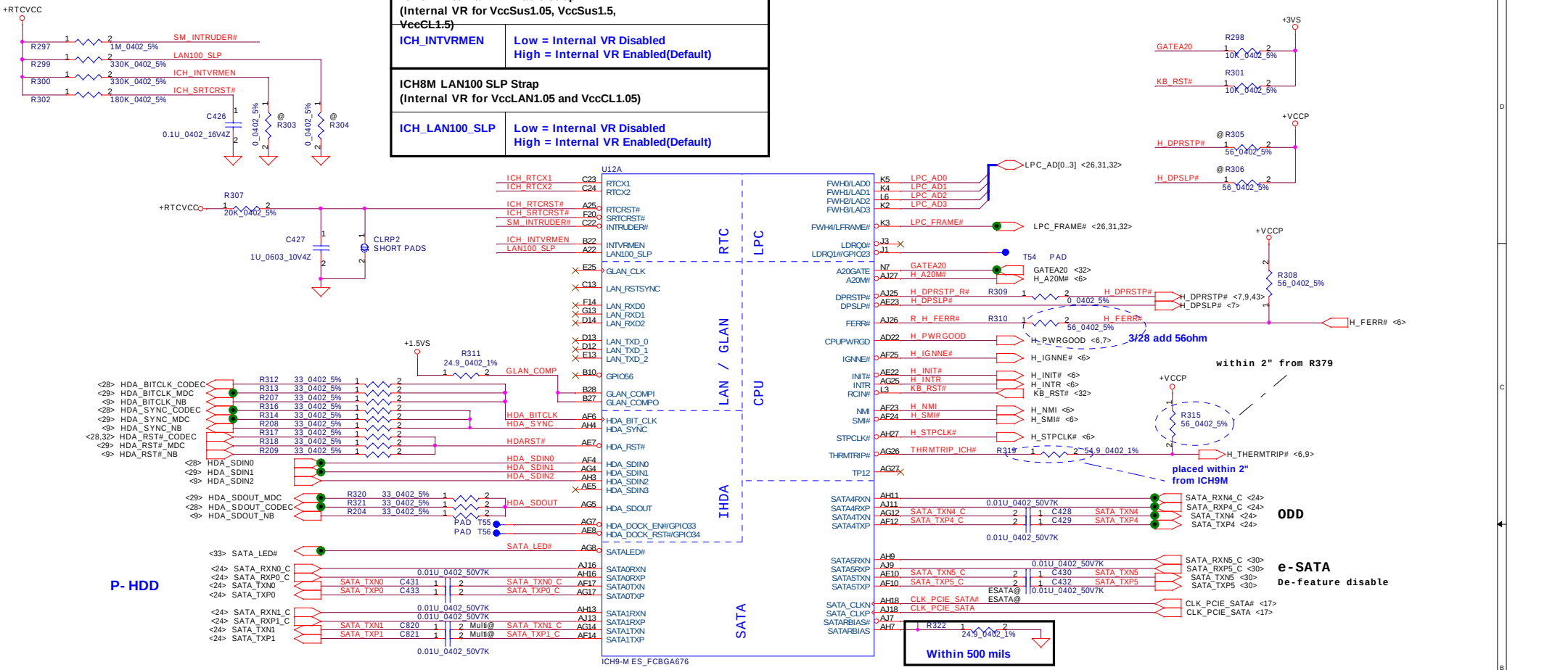
Compal Electronics, Inc.			
Title	ICH9(1/4)-PCI/INT		
Size	Document Number	Montevina Blade UMA LA4101P	Rev 0.3
Date: Saturday, January 05, 2008	Sheet 20 of 46		

ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)

ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	

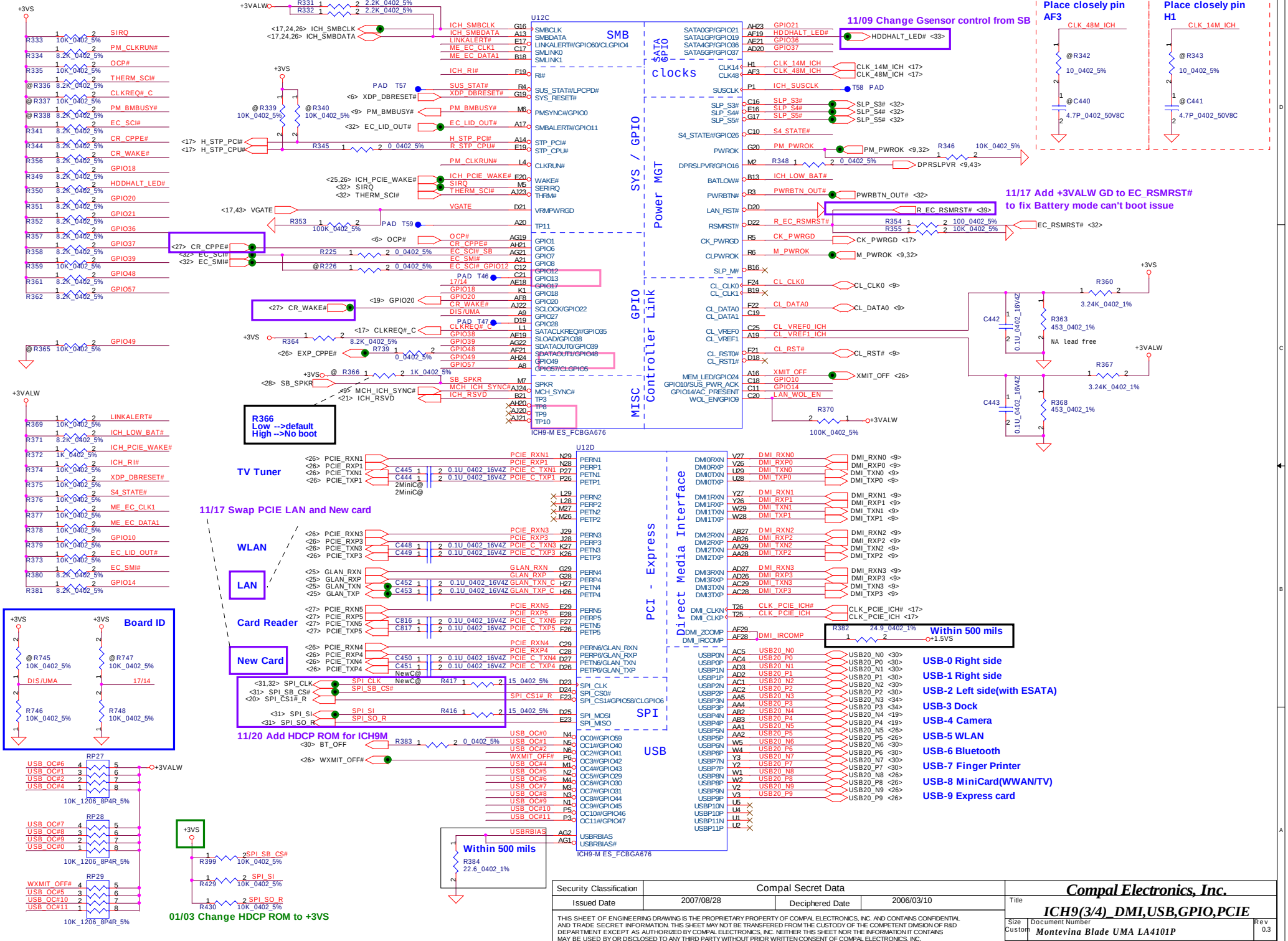
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **ICH9(2/4)_LAN,HD,IDE,LPC**

Size	Document Number	Rev
Custom	Montevina Blade UMA LA4101P	0.3

Date: Saturday, January 05, 2008 | Sheet 21 of 46



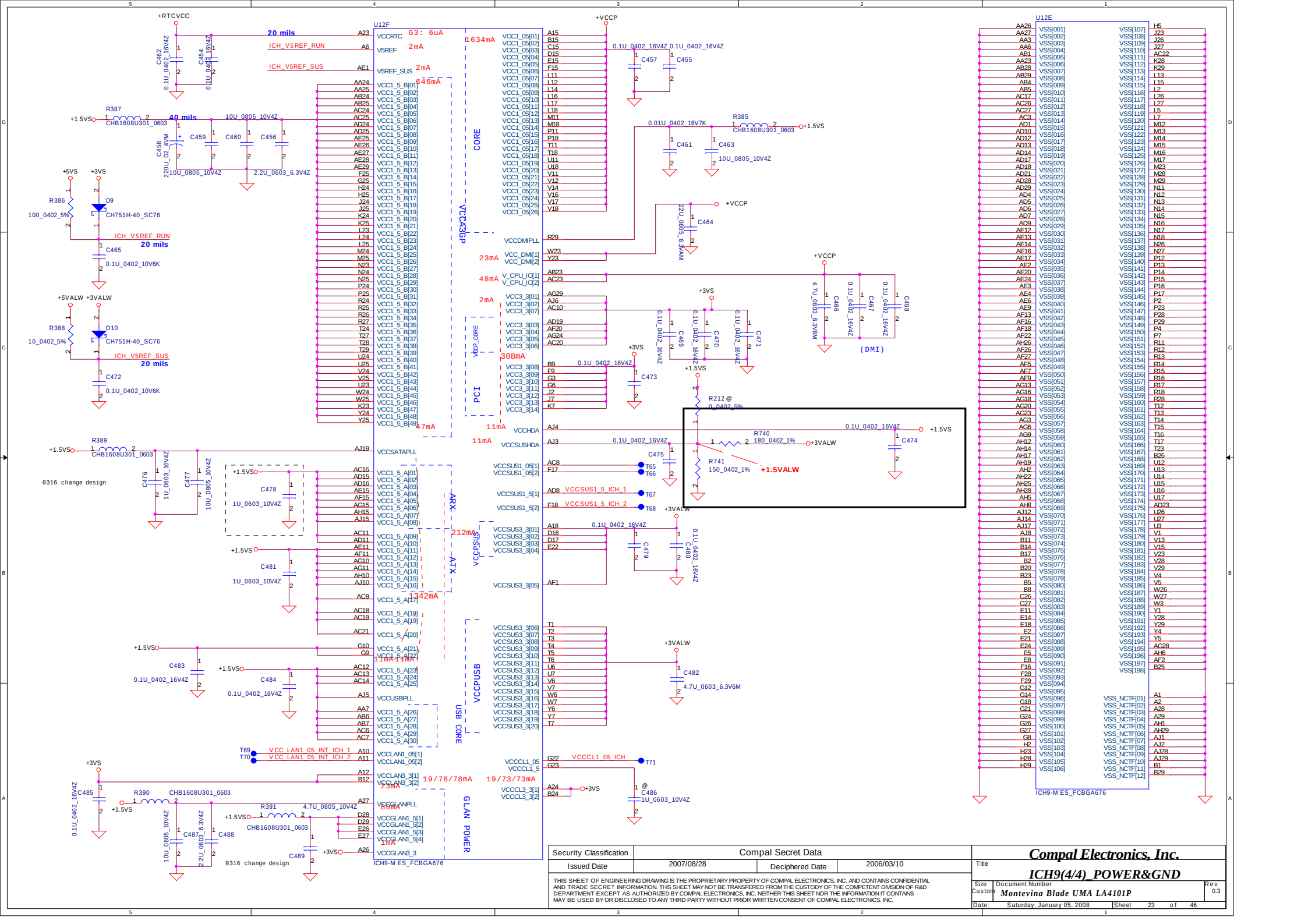
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: ICH9(3/4)_DMI,USB,GPIO,PCIE

Size	Document Number	Rev
Custom	Montevina Blade UMA LA4101P	0.3

Date: Saturday, January 05, 2008 | Sheet 22 of 46


U12F
ICH9-M ES_FCBGA676
U12E
ICH9-M ES_FCBGA676
CORE
VCCA3GP
PCI
VCCP_CORE
ARX
ATX
VCCPSUS
USB CORE
VCCPUSB
GLAN POWER
(DMI)
0316 change design
0316 change design
+RTCVCC
+1.5VS
+5VS
+3VS
+5VALW
+3VALW
+1.5VALW
+VCCP
20 mils
40 mils
ICH_V5REF_RUN
ICH_V5REF_SUS
VCC_LAN1_05_INT_ICH_1
VCC_LAN1_05_INT_ICH_2
VCCCL1_05_ICH
VCCSUS1_5_ICH_1
VCCSUS1_5_ICH_2
G3: 6uA
2mA
646mA
1634mA
23mA
48mA
2mA
308mA
11mA
11mA
47mA
212mA
1242mA
11mA
11mA
19/78/78mA
19/73/73mA
2.3mA
80mA
1mA
R387 CHB1608U301_0603
R386 100_0402_5%
R388 10_0402_5%
R389 CHB1608U301_0603
R390 CHB1608U301_0603
R391 CHB1608U301_0603
R385 CHB1608U301_0603
R212 @ 0_0402_5%
R740 180_0402_1%
R741 150_0402_1%
D9 CH751H-40_SC76
D10 CH751H-40_SC76
C462 0.1U_0402_16V4Z
C454 0.1U_0402_16V4Z
C458 220U_D2_4VM
C459 10U_0805_10V4Z
C460
C456 2.2U_0603_6.3V4Z
C465 0.1U_0402_10V6K
C472 0.1U_0402_10V6K
C476 1U_0603_10V4Z
C477 10U_0805_10V4Z
C478 1U_0603_10V4Z
C481 1U_0603_10V4Z
C483 0.1U_0402_16V4Z
C484 0.1U_0402_16V4Z
C485 0.1U_0402_16V4Z
C486 1U_0603_10V4Z
C487 2.2U_0603_6.3V4Z
C488
C489
C457 0.1U_0402_16V4Z
C455 0.1U_0402_16V4Z
C461 0.01U_0402_16V7K
C463 10U_0805_10V4Z
C464 22U_0805_6.3V4M
C466 4.7U_0603_6.3V6M
C467 0.1U_0402_16V4Z
C468 0.1U_0402_16V4Z
C469 0.1U_0402_16V4Z
C470 0.1U_0402_16V4Z
C471 0.1U_0402_16V4Z
C473 0.1U_0402_16V4Z
C474 0.1U_0402_16V4Z
C475
C479
C480 0.1U_0402_16V4Z
C482 4.7U_0603_6.3V6M
T65
T66
T67
T68
T69
T70
T71
Security Classification
Compal Secret Data
Issued Date
2007/08/28
Deciphered Date
2006/03/10
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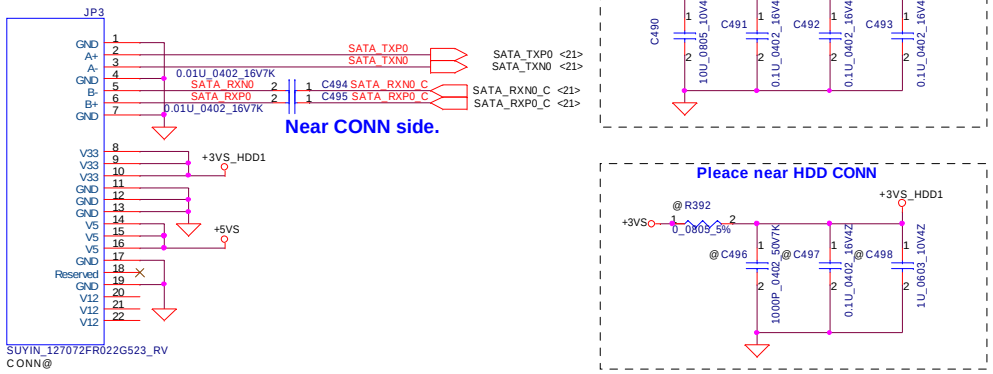
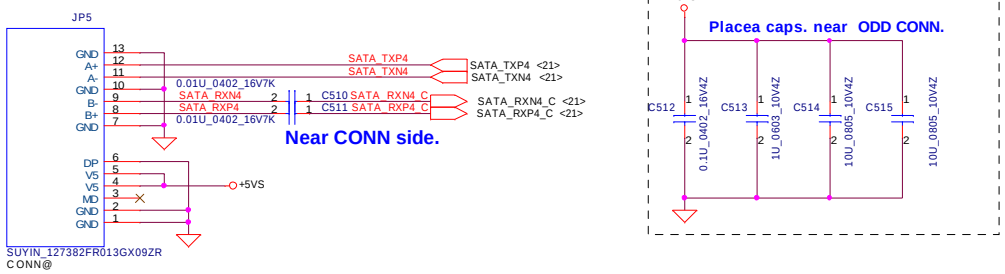
Compal Electronics, Inc.
Title
ICH9(4/4)_POWER&GND
Size
Custom
Document Number
Montevina Blade UMA LA4101P
Rev
0.3
Date:
Saturday, January 05, 2008
Sheet
23
of
46

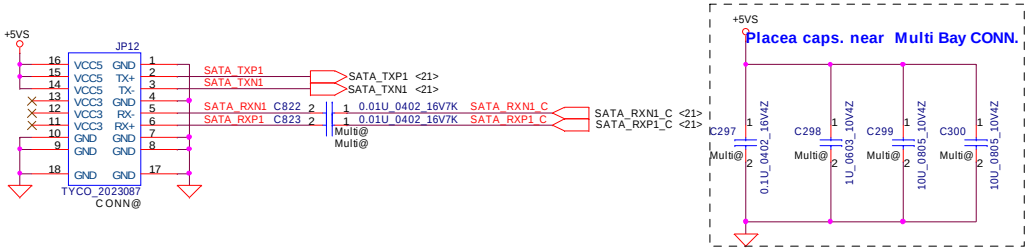
HDD Connector



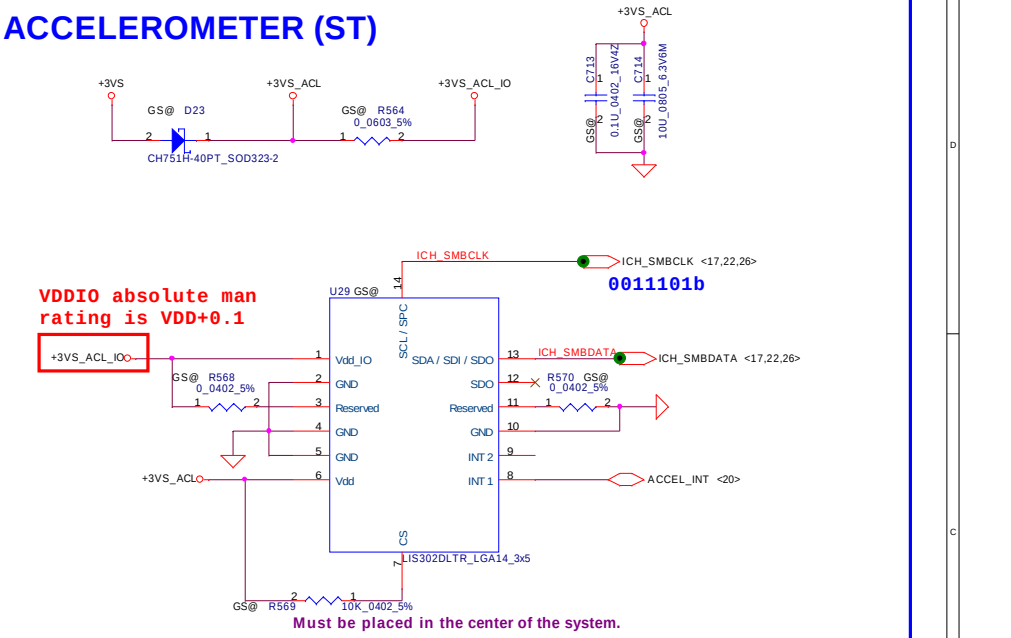
CD-ROM Connector



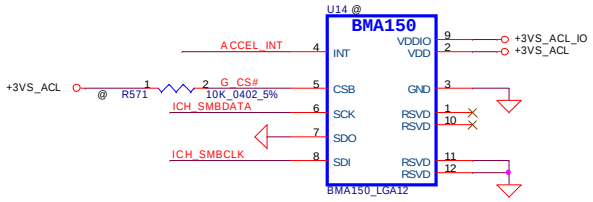
Multi Bay



ACCELEROMETER (ST)



ACCELEROMETER (Bosch)



ZZZ2
PCB-MB

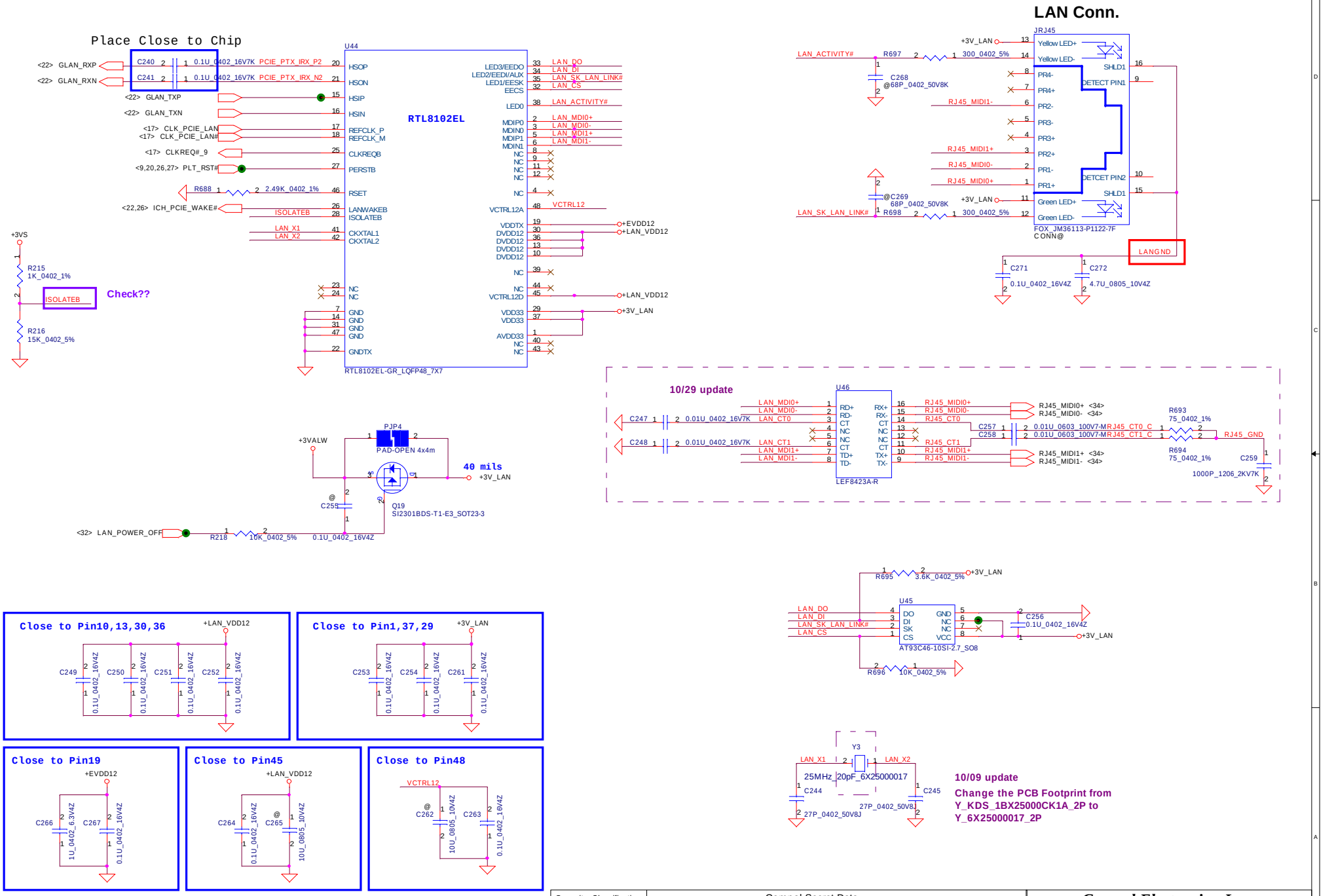
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: HDD & CDROM

Size: Custom | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 24 of 46



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2007/06/30

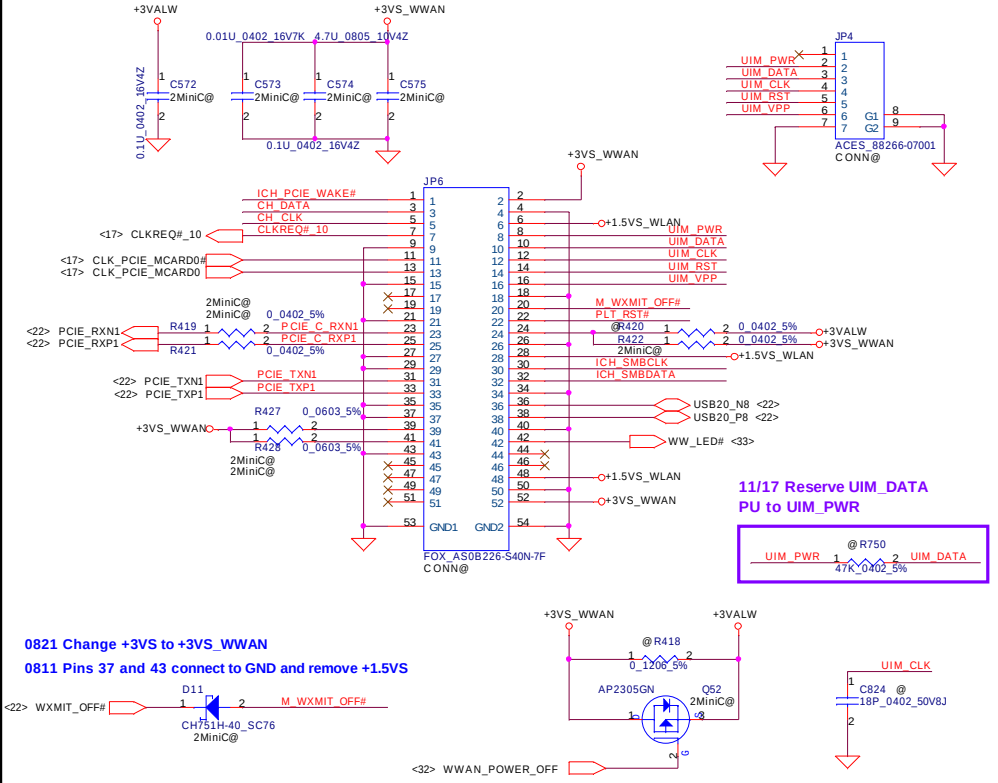
Compal Electronics, Inc.

Title: RTL8102EL LAN

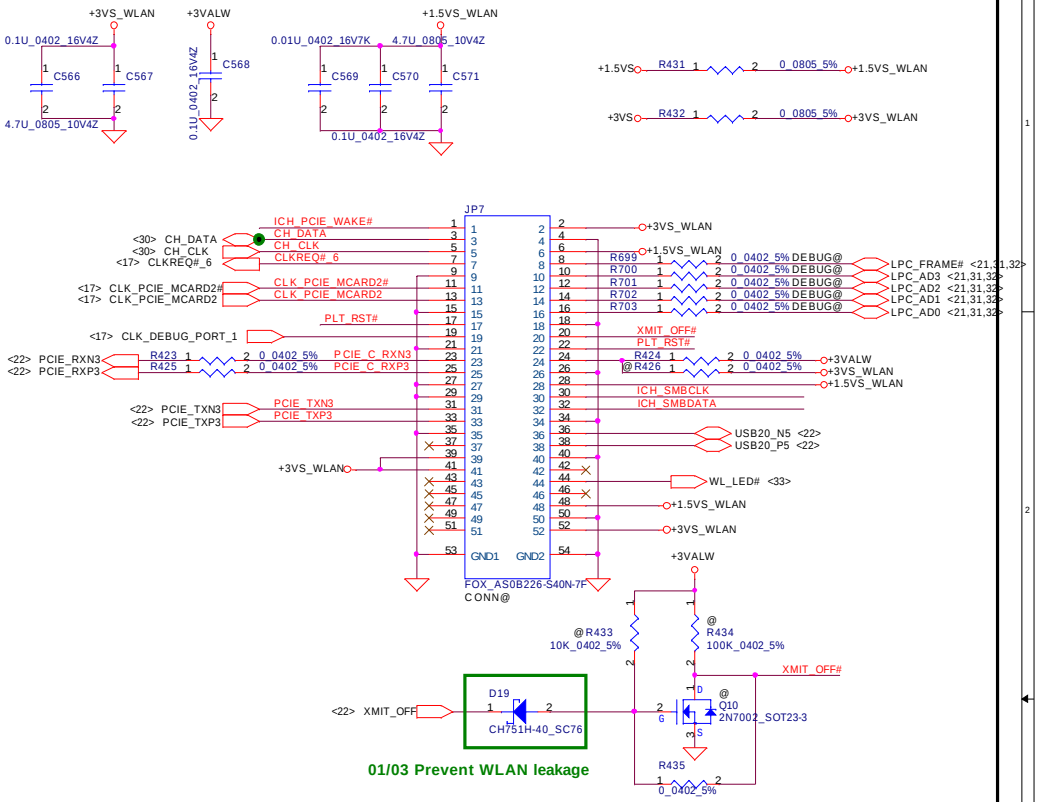
Size: Custom | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 25 of 46

Mini Card 0--TV tuner/WWAN/Robson

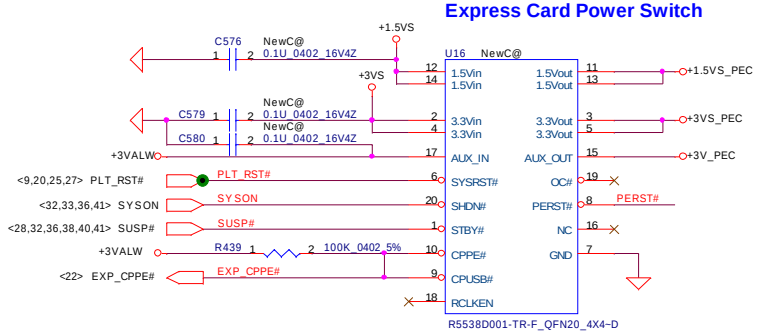


Mini Card 2---WLAN



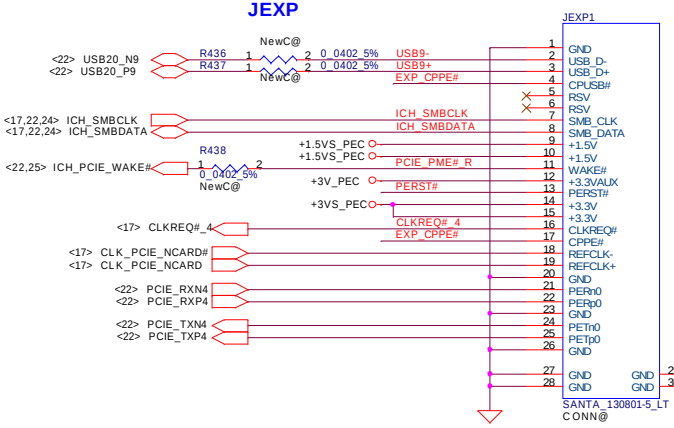
New Card

Express Card Power Switch

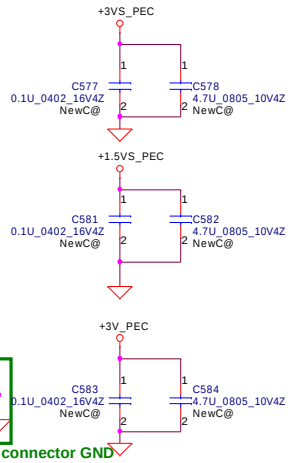


internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

Close to JEXP



Near to Express Card slot.



01/03 New card PTH connector GND

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **WLAN, WWAN, New Card**

Size | Document Number: **Montevina Blade UMA LA4101P** | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 26 of 46

09/26 (JMicron)recommend C1328/1000pF close to U36 pin5
09/26 (JMicron)recommend place C1329/0.1uF near by C1328
09/26 (JMicron)recommend (APVDD, 20 mil width, less than 120mil long)

09/26 (JMicron)recommend width/length: 12mil / <250mil for PREXT signal (pin 7)

11/07 Change to 10K(vender)

01/03 Change Cardreader LED control

09/26 (JMicron)recommend add a test point for pin 13、14

11/07 Change to 8.2K(vender)

11/09 Add D18 for cardreader wake up

use for PWR_EN#

8mA sink current

11/07 Stuff for JMB385 internal LDO

Use 0603 type and over 20 mils trace width on both side

09/26 (JMicron)recommend change to 0805 Size

09/26 (JMicron)recommend +VCC_OUT >30mil

reserved power circuit

11/07 Change U37 correct PCBFootprint SOT23

11/07 BOM delete for JMB385 internal LDO

09/26 Must change P mos FET

11/07 Don't stuff for JMB385 internal LDO

White LED: VF=3V, IF = 5mA, Res = 56ohm

11/09 don't support DIM function

01/03 Change Cardreader LED control

Card Reader Connector

11/17 Update CIS library

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/10/06

Compal Electronics, Inc.

Title: USB CardReader&CONN

Size: Custom | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 27 of 46

CODEC POWER

(4.75V(4.56~4.94V))
300mA

+1.5VS_HDA → R1051 BLM18BD601SN1D_0603 → +1.5VS
C1342 0.1U_0402_16V4Z

+3VS → R1052 BLM18BD601SN1D_0603 → +3VDD_CODEC
C1337 1U_0603_10V4Z
C1338 0.1U_0402_16V4Z

+VDDA_CODEC_R → R1053 0_0805_5% → +VDDA_CODEC
C1339 0.1U_0402_16V4Z
C1340 1U_0603_10V4Z

W=40Mil
+5VALW → C1341 0.1U_0402_16V4Z → U39 IN
<26,32,36,38,40,41> SUSP# → U39 SHDN
U39 GND
U39 OUT → +VDDA_CODEC
U39 BYP → C1344 0.1U_0402_16V4Z
C1343 2.2U_0805_16V4Z
U39: G9191-475T1U_SOT23-5

11/07 Change to 4.75V LDO

U38 (92HD71B7X5NLGXA1X8_QFN48_7X7)

+3VDD_CODEC	9	DVDD_CORE*	
	1	DVDD_CORE	
+VDDA_CODEC_R	25	AVDD1*	
	38	AVDD2**	
+1.5VS_HDA	3	DVDD_IO	
	32	MONO_OUT	
<21> HDA_BITCLK_CODEC	6	BITCLK	
<21> HDA_SDOUT_CODEC	5	SDO	
<21> HDA_SDIN0	8	SDI_CODEC	
<21> HDA_SYNC_CODEC	10	SYNC	
<21,32> HDA_RST#_CODEC	11	RESET#	
<19> DMIC_CLK	46	DMIC_CLK	
<22> SB_SPKR	33	CAP2	
	12	PCBEEP	
	40	NC / OTP	
<34> SENSE_B#	34	SENSE_B / NC	
	37	NC	
	18	NC	
	19	NC	
	20	NC	
C1355 10U_0805_10V4Z	27	VREFFILT	
	26	AVSS1*	
	42	AVSS2**	
	7	DVSS**	
EAPD/ SPDIF OUT 0 or 1 / GPIO 0	47	EAPD_CODEC	EAPD_CODEC <32>
VOL_UP/DMIC_0/GPIO 1	2		DMIC_DAT <19>
VOL_DN/DMIC_1/GPIO 2	4		
GPIO 3	30		
VREFOUT-E / GPIO 4	31		
GPIO 5	43		
GPIO 6	44		
SPDIF OUT1 / GPIO 7	45	SPDIF_OUT	SPDIF_OUT <34>
SPDIF OUT0	48		
	28	VREFOUT_B	VREFOUT_B <29>
VREFOUT-C	29		
SENSE_A	13	SENSE	
PORTA_R	41	HP_OUTR	HP_OUTR <29>
PORTA_L	39	HP_OUTL	HP_OUTL <29>
PORTB_R	22	MIC_EXTR	MIC_EXT_R <29>
PORTB_L	21	MIC_EXTL	MIC_EXT_L <29>
PORTC_R	24	MIC_INR	
PORTC_L	23	MIC_INL	
PORTD_R	36	LINE_OUT_R	LINE_OUT_R <29>
PORTD_L	35	LINE_OUT_L	LINE_OUT_L <29>
PORTE_R	15	DOCK_MICR	
PORTE_L	14	DOCK_MICL	
PORTF_R	17		
PORTF_L	16		

11/09 reserve EC_BEEP

@R445 47K_0402_5%
<32> EC_BEEP → EC_BEEP

HDA_BITCLK_CODEC
@R1054 47_0402_5%
@C1345 33P_0402_50V8K

R1055 33_0402_5% HDA_SDIN0_CODEC
HDA_SYNC_CODEC
HDA_RST#_CODEC

R1058 22_0402_5%
R1060 47K_0402_5%
C1347 1U_0603_10V4Z
R1061 10K_0402_5%
C1348 MONO_INR 0.1U_0402_16V4Z
C1349 0.1U_0402_16V4Z

R1062 5.1K_0402_1%
R1063 39.2K_0402_1%
C1353 0.1U_0402_16V4Z

C1355 10U_0805_10V4Z
VC_REFA

SPDIF_OUT <34>
01/03 Change SPDIF to SPDIF1

+VDDA_CODEC_R
R1056 5.1K_0402_1%
R1057 20K_0402_1%
R1059 39.2K_0402_1%
R683 10K_0402_1%
C1346 0.1U_0402_16V4Z
EXTMIC_DET# <29>
JACK_DET# <29,34>
INTMIC_DET# <29>
11/07 Change R1059 39.2K

HP Jack & Dock

Jack MIC
C1350 1U_0603_10V6K
C1351 1U_0603_10V6K
C1352 0.022U_0402_16V7K → MIC_IN_R <29>

11/08 Change C1352、C1354 (recommend)
Internal MIC
@R1064 0_0603_5%
C1354 0.022U_0402_16V7K → MIC_IN_L <29>

Internal SPKR.

DOCK MIC
C1356 1U_0603_10V6K
C1357 1U_0603_10V6K
R733 10K_0402_5% → DOCK_MIC_R <34>
R734 10K_0402_5% → DOCK_MIC_L <34>

R735 1.21K_0402_1%
R736 1.21K_0402_1%
1/10*Vin need close to Codec

@C1358 0.1U_0402_16V4Z
@C1359 0.1U_0402_16V4Z
@C1360 0.1U_0402_16V4Z
@C1361 0.1U_0402_16V4Z
C1362 0_0402_5%
R1065 0_1206_5%
R596 0_1206_5%
GNDA <29,34>

GND GNDA

11/07 Stuff 0 Ohm for AGND and GND

SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

Title: Codec_IDT9271B7
Size: Custom | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3
Date: Saturday, January 05, 2008 | Sheet 28 of 46

GAIN0	GAIN1	Av(inv)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

11/17 Change to15.6 dB

SPEAKER

11/07Change JP60 PCB Footprint from ACES_85204-04001_4P to ACES_88231-04001_4P

8/31EMI request

Audio/B & CIR

HP OUT

HP OUT For Docking

11/07 Add Capacitor avoid DC lever to Docking audio

HP OUT For M/B

EXTMIC IN

INTMIC IN

MDC 1.5 Conn.

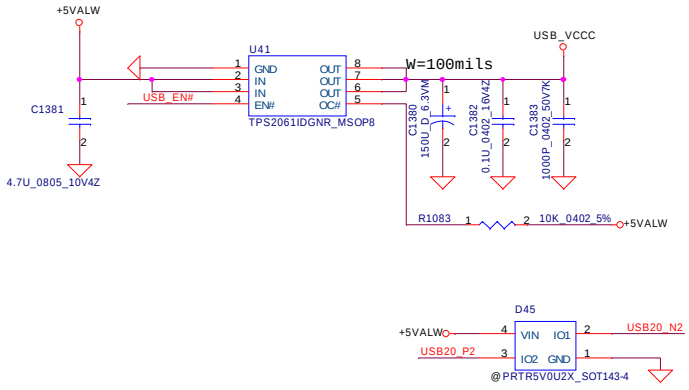
Connector for MDC Rev1.5

MDC Standoff

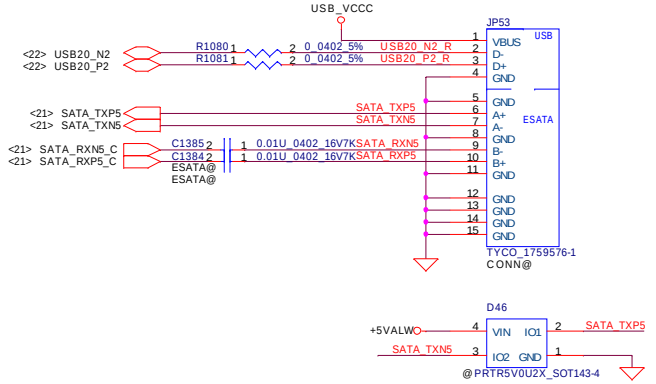
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Title	AMP & Audio Jack		
Size	Custom	Document Number	Montevina Blade UMA LA4101P
Rev	0.3		
Date:	Saturday, January 05, 2008	Sheet	29 of 46

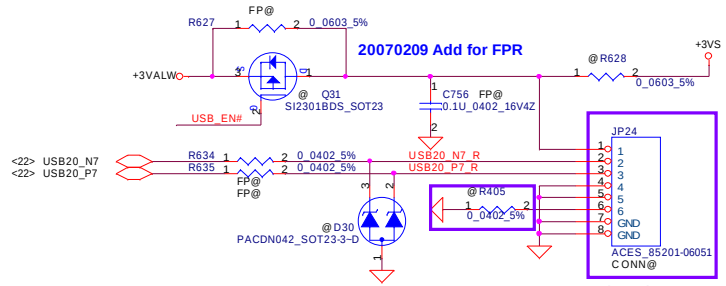
Left side USB Connector



Left side ESATA/USB combination Connector

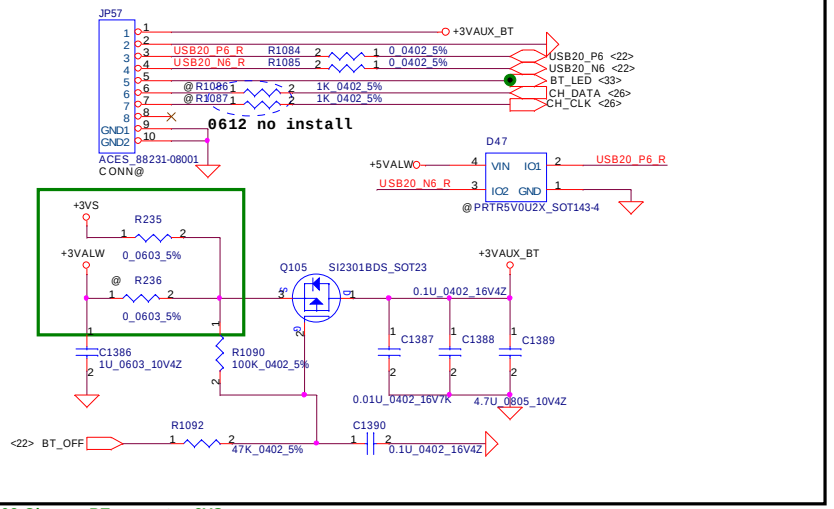


Finger printer



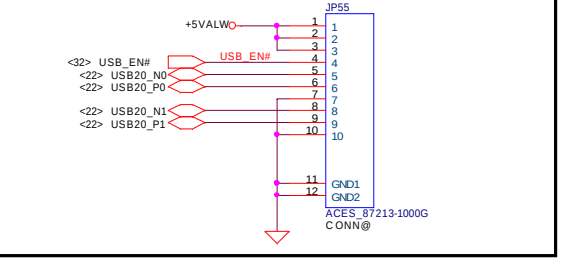
BT Connector

Need change to New version



01/03 Change BT power to +3VS

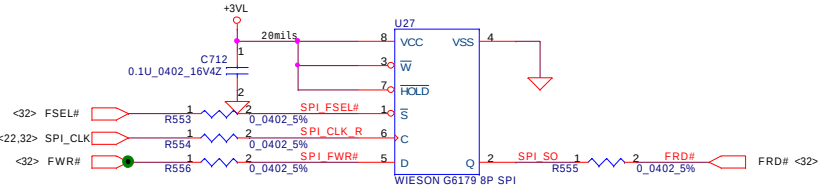
USB cable connector for Right side



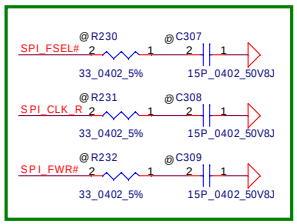
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: USB, BT, eSATA			
Size	Document Number: Montevina Blade UMA LA4101P		Rev: 0.3
Date: Saturday, January 05, 2008	Sheet 30 of 46		

SPI ROM

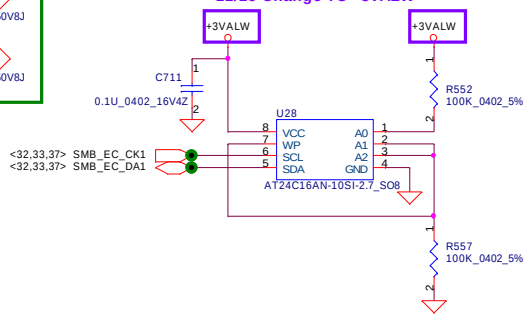


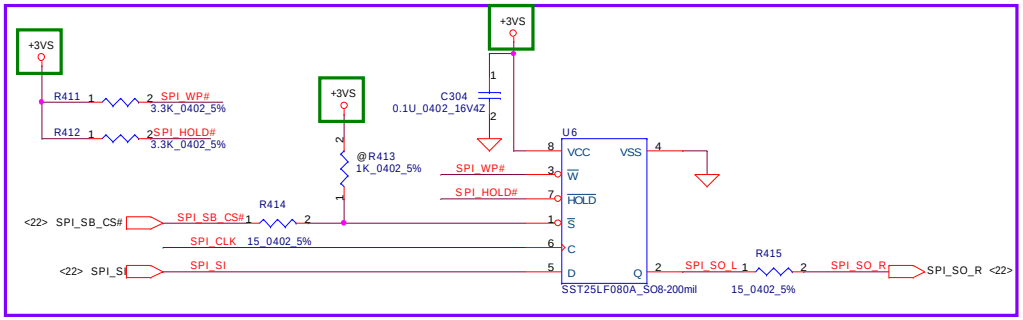
SP07000F500 S SOCKET WIESON G6179-100000 8P SPIFLASH
WIESO_G6179-100000_8P



12/27EMI request

11/16 Change TO +3VALW



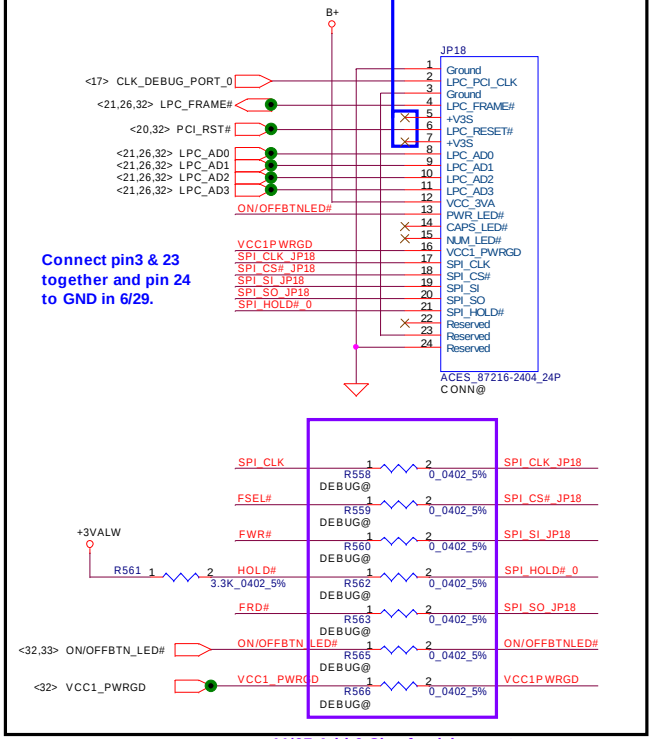


11/17 Add SB HDCP ROM

01/03 Change HDCP ROM to +3VS

LPC Debug Port

Change from +3VL to +3VS. 6/9
Removed +3VS. 6/13



11/07 Add 0 Ohm for debug port

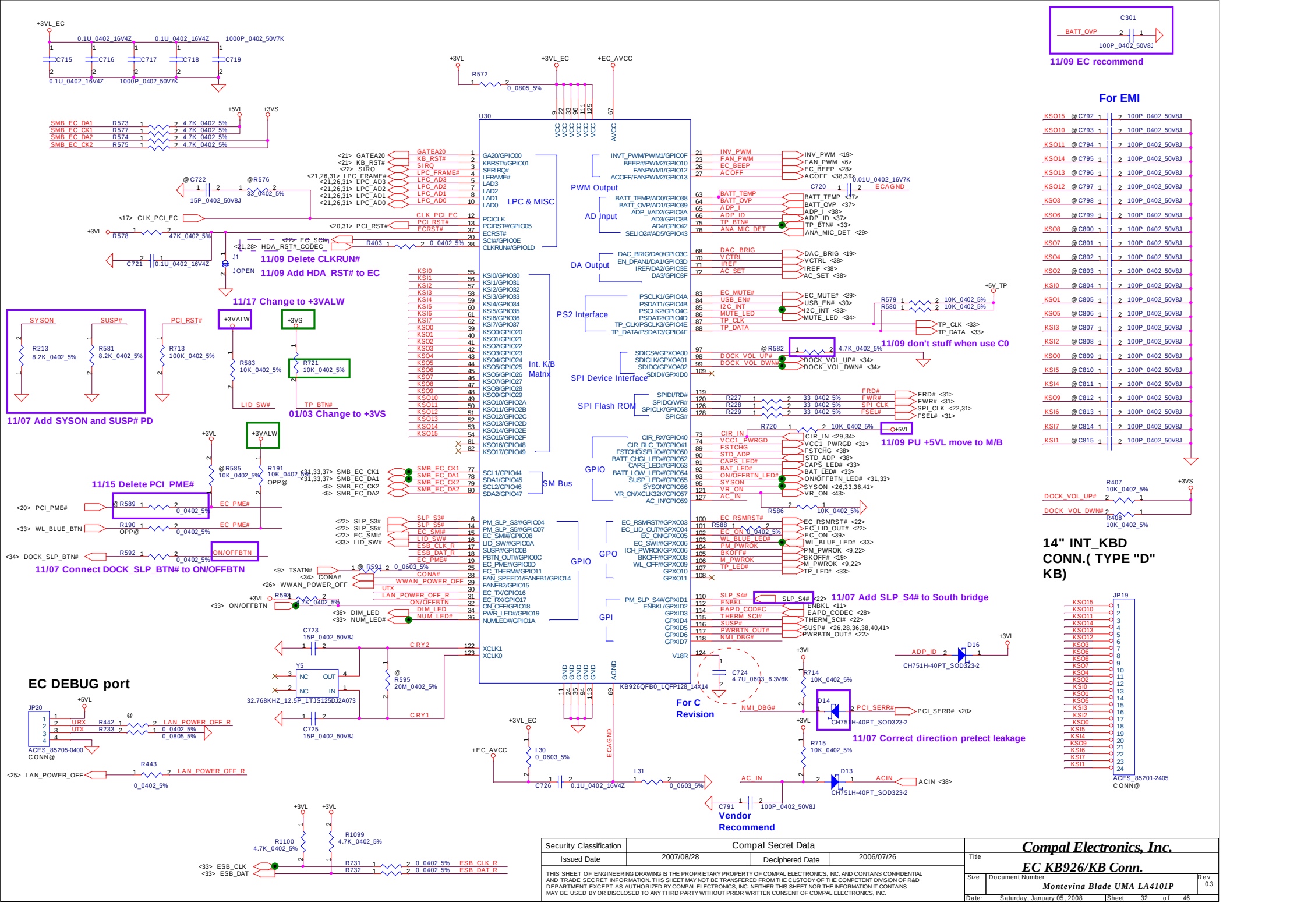
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: BIOS ROM

Size | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 31 of 46



Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

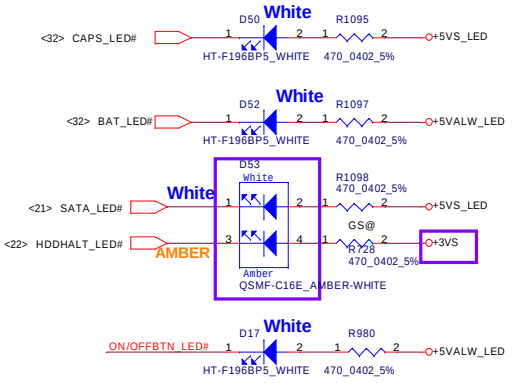
Compal Electronics, Inc.

Title: **EC KB926/KB Conn.**

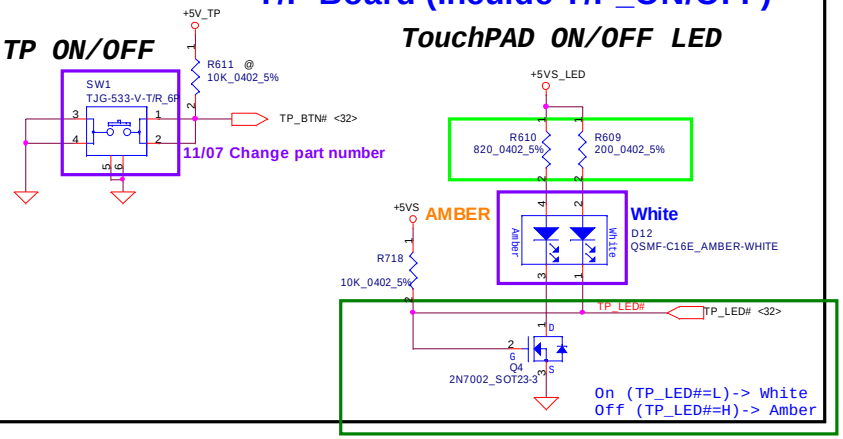
Size	Document Number	Rev
	Montevina Blade UMA LA4101P	0.3

Date: Saturday, January 05, 2008 Sheet 32 of 46

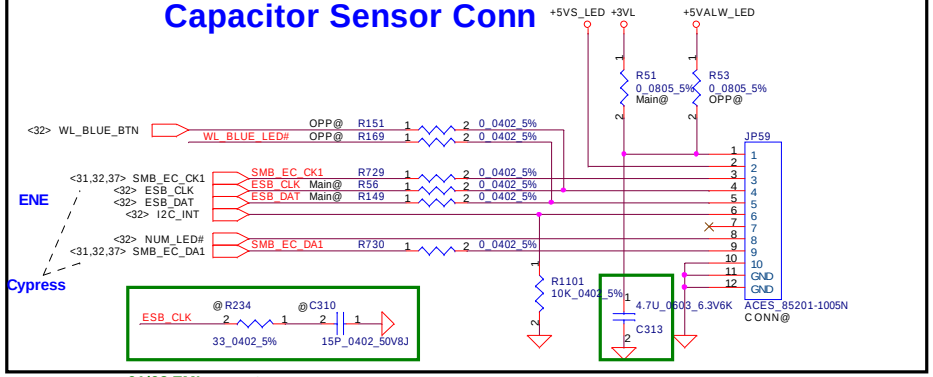
System LED



T/P Board (Inculde T/P_ON/OFF)

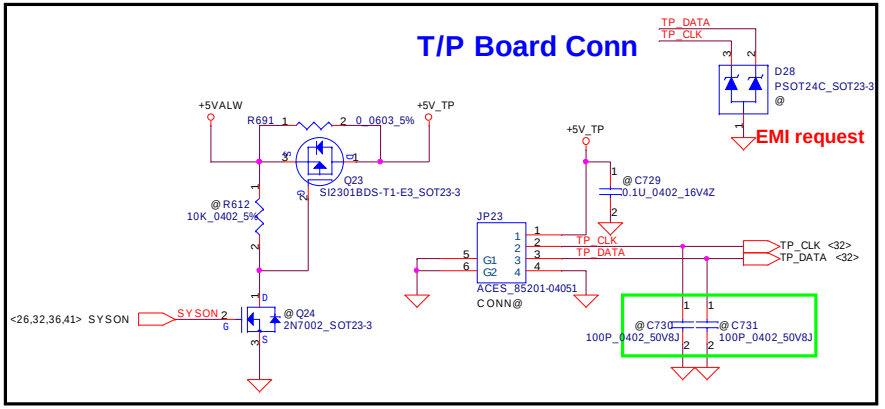


Capacitor Sensor Conn

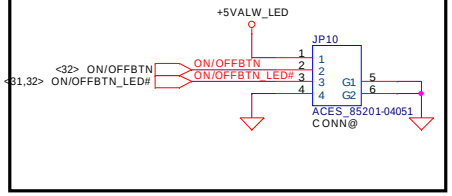


01/03 EMI request

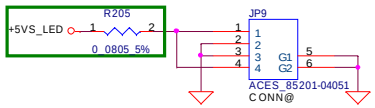
T/P Board Conn



ON/OFF Button Connector

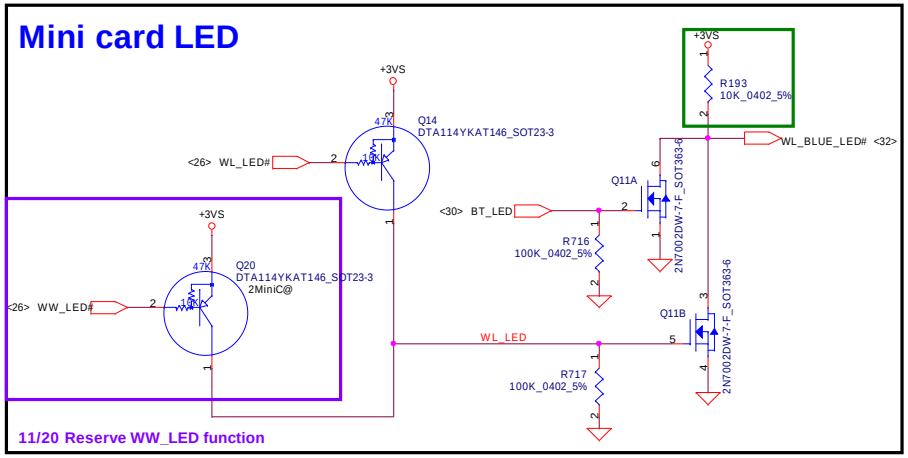


Keyboard backlight Conn

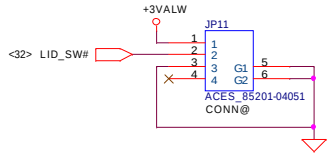


01/03 Keyboard backlight reserve a 0805 size resistor

Mini card LED



Lid Switch Connector



01/03 Change Lid switch connector type

Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

Compal Electronics, Inc.

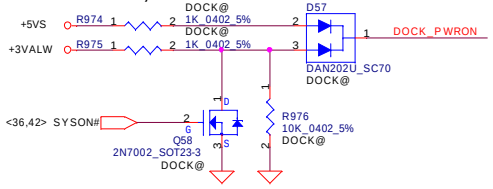
Title: KBD, ON/OFF, SW, CIR

Size | Document Number: Montevina Blade UMA LA4101P | Rev 0.3

Date: Saturday, January 05, 2008 | Sheet 33 of 46

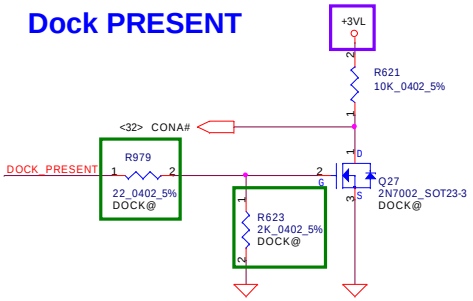
Atlas/ Saturn Dock

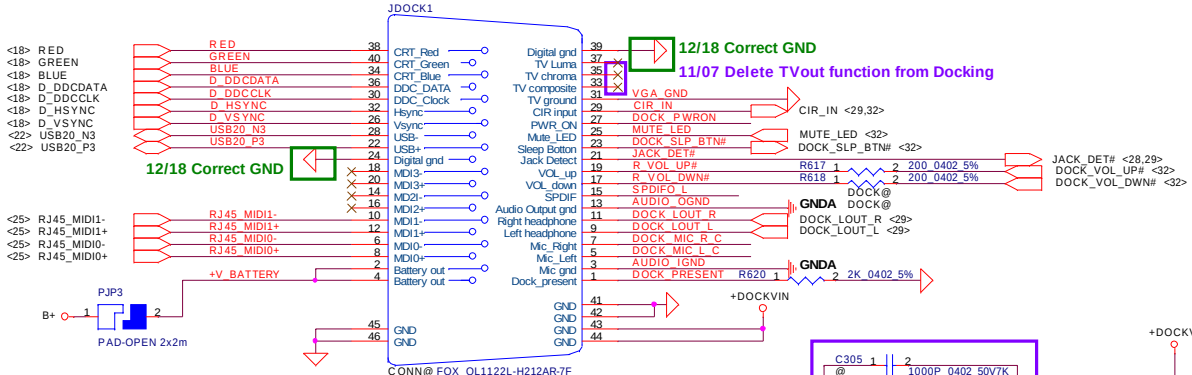
DOCK_PWR_ON Spec
0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on

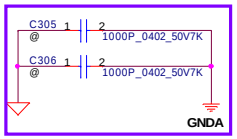


Dock PRESENT

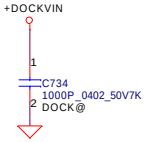
11/12 Change to +3VL





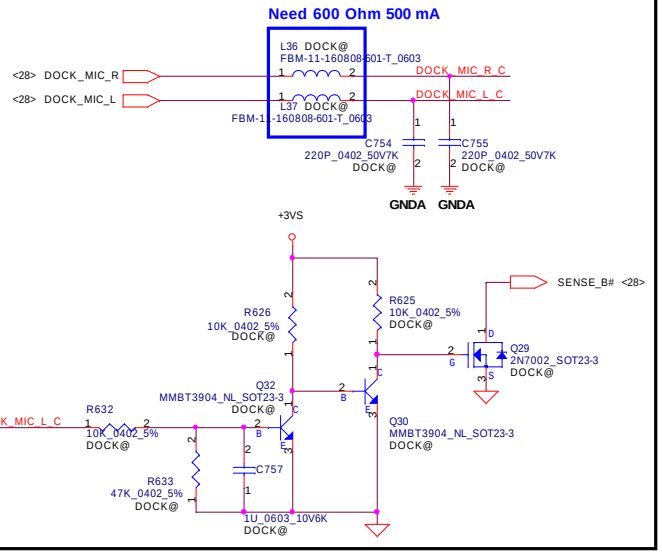


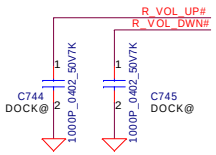
11/17 Reserve

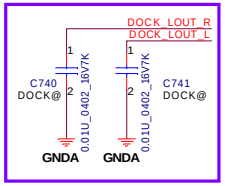


MIC_Dock

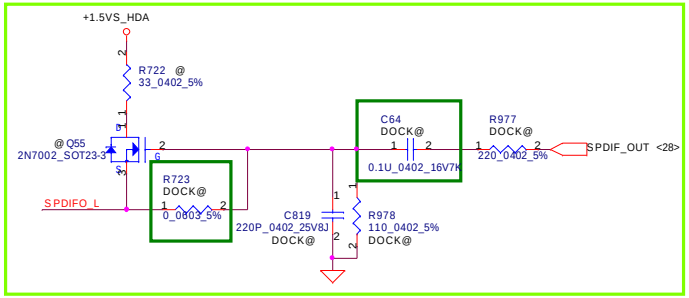
Need 600 Ohm 500 mA







11/17 Recommend



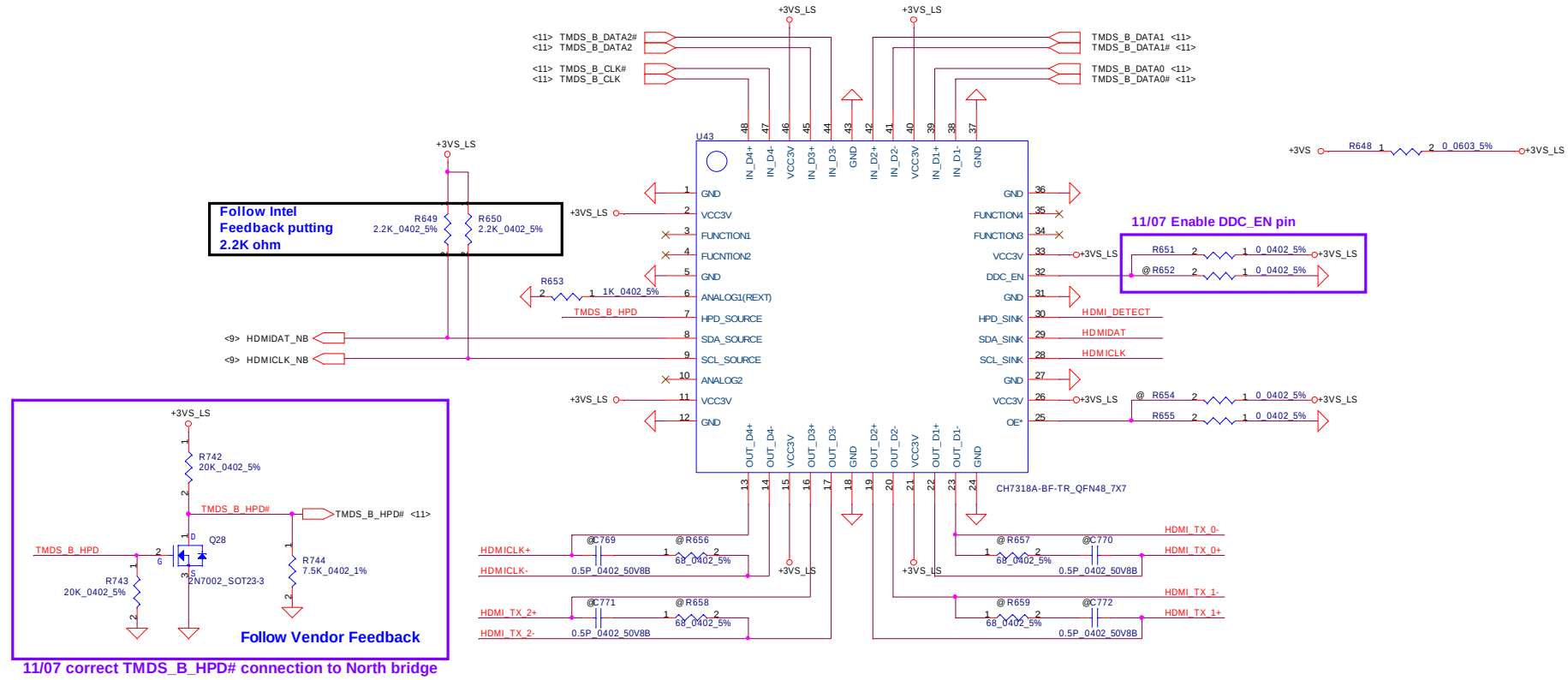
Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

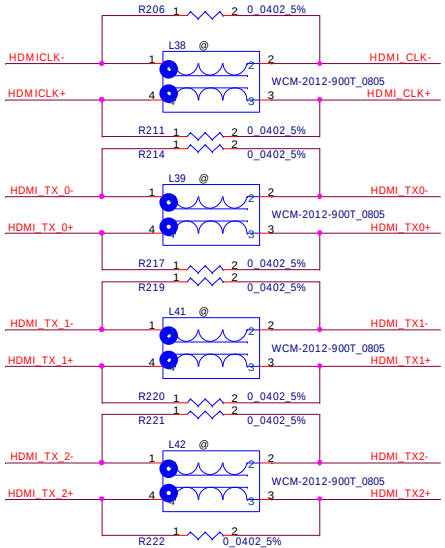
Compal Electronics, Inc.

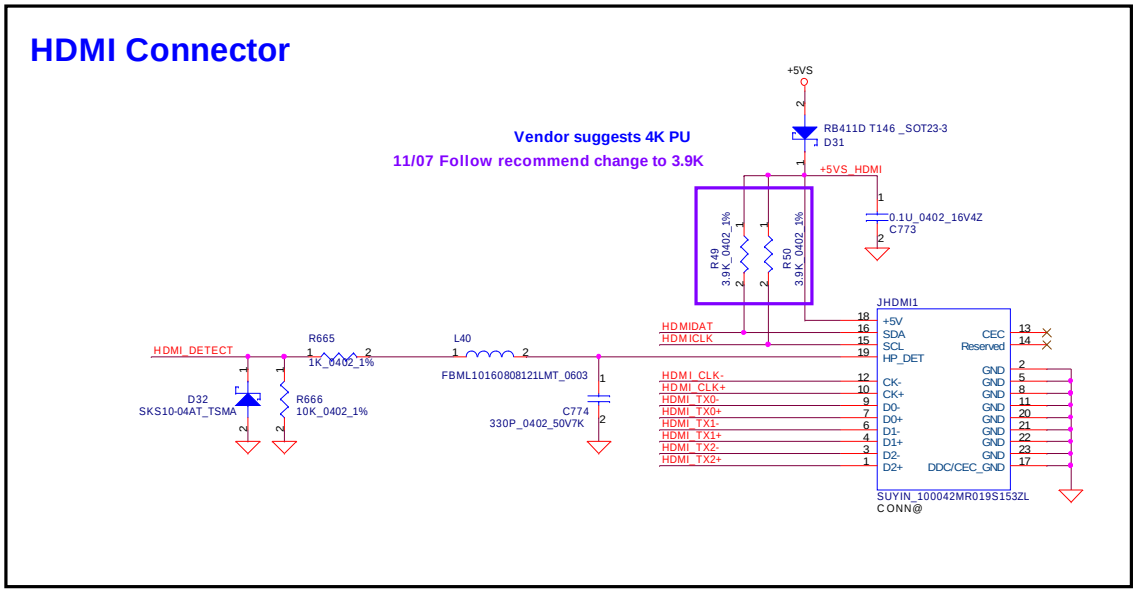
Title: **DOCK CONN.**

Size	Document Number	Rev
Custom	Montevina Blade UMA LA4101P	0.3

Date: Saturday, January 05, 2008 Sheet 34 of 46



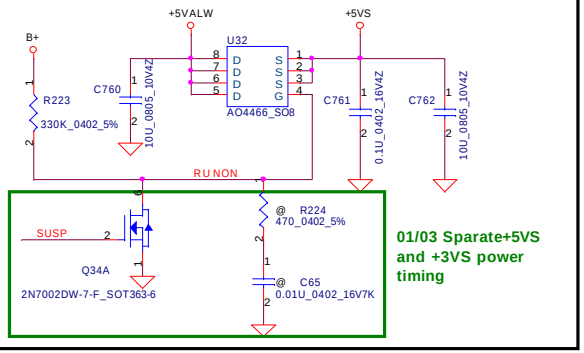




Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/03/10

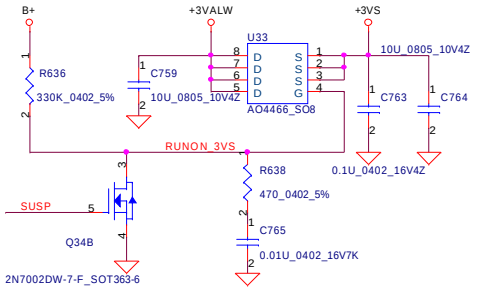
Compal Electronics, Inc.			
Title: HDMI LS & Conn.			
Size: Custom	Document Number: Montevina Blade UMA LA4101P		Rev: 0.3
Date: Saturday, January 05, 2008	Sheet 35 of 46		

+5VALW to +5VS Transfer

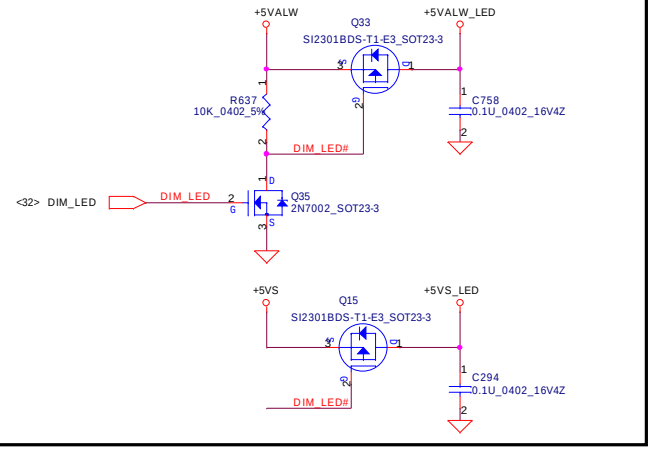


01/03 Sparate+5VS and +3VS power timing

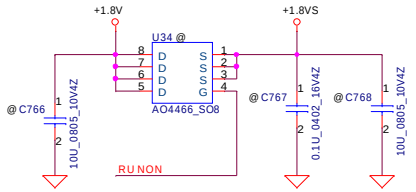
+3VALW to +3VS Transfer



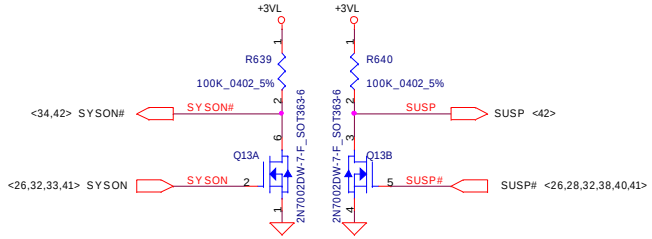
DIM LED



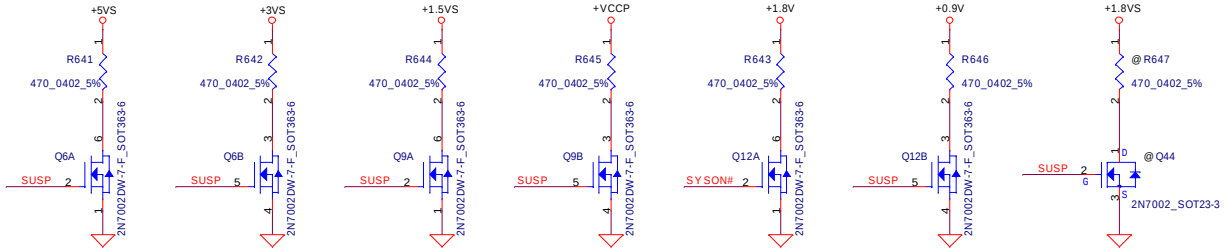
+1.8V to +1.8VS Transfer

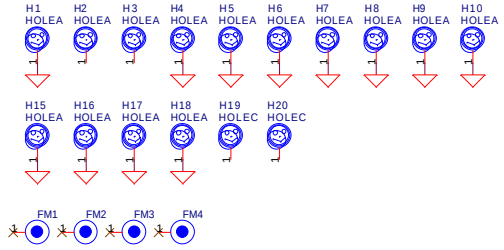


11/07 BOM Delete +1.8VS for Cardreader internal LDO



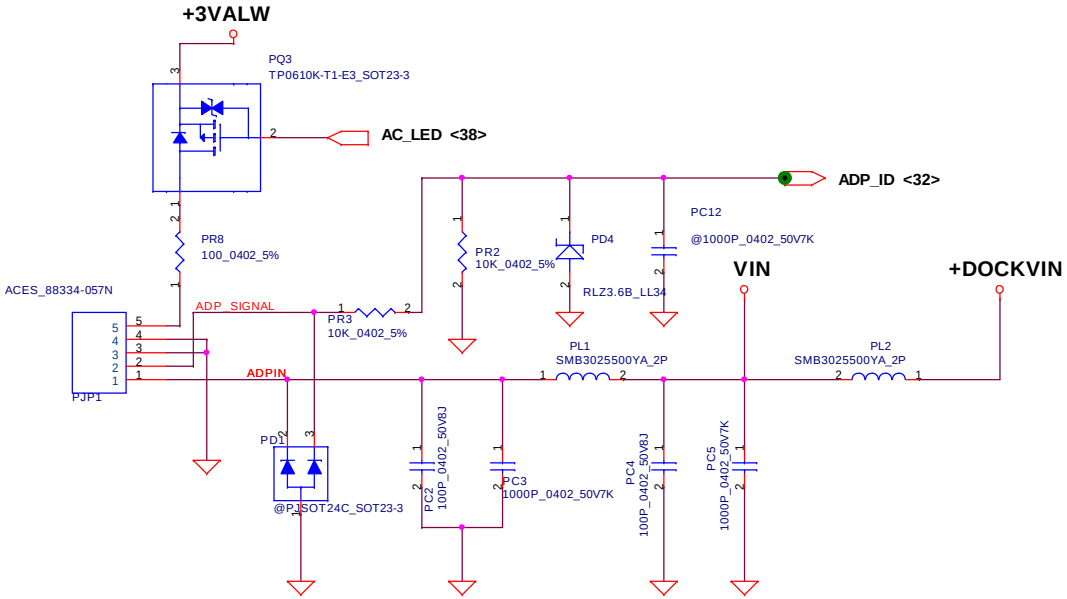
Discharge circuit

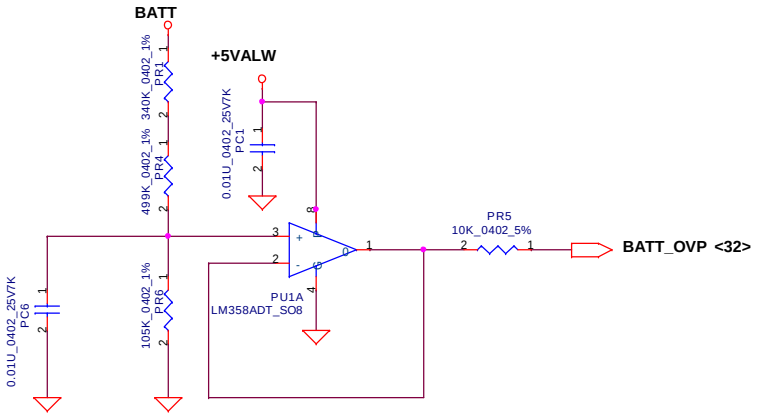


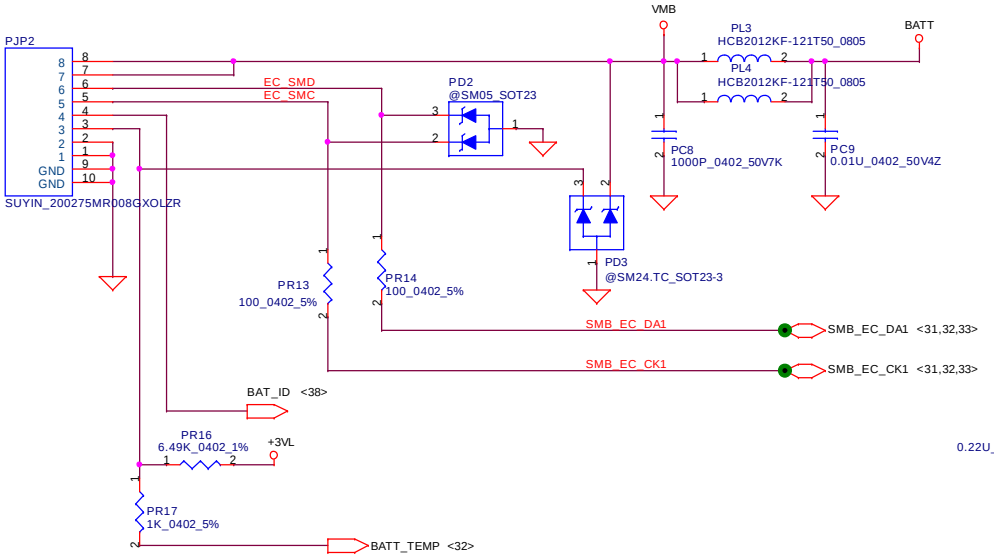


Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/07/26

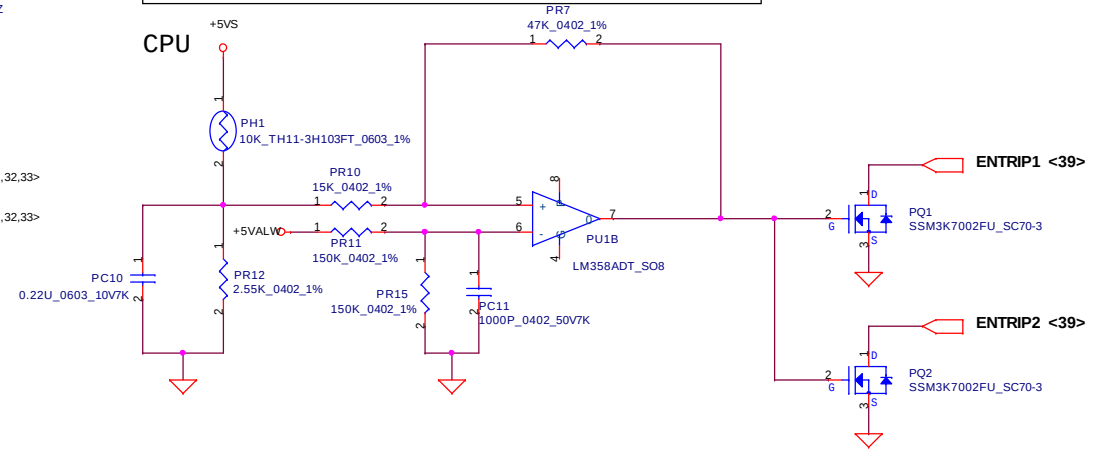
Compal Electronics, Inc.			
Title: DC/DC Interface			
Size	Document Number: Montevina Blade UMA LA4101P		Rev: 0.3
Date: Saturday, January 05, 2008	Sheet 36 of 46		







PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 47 +-3 degree C



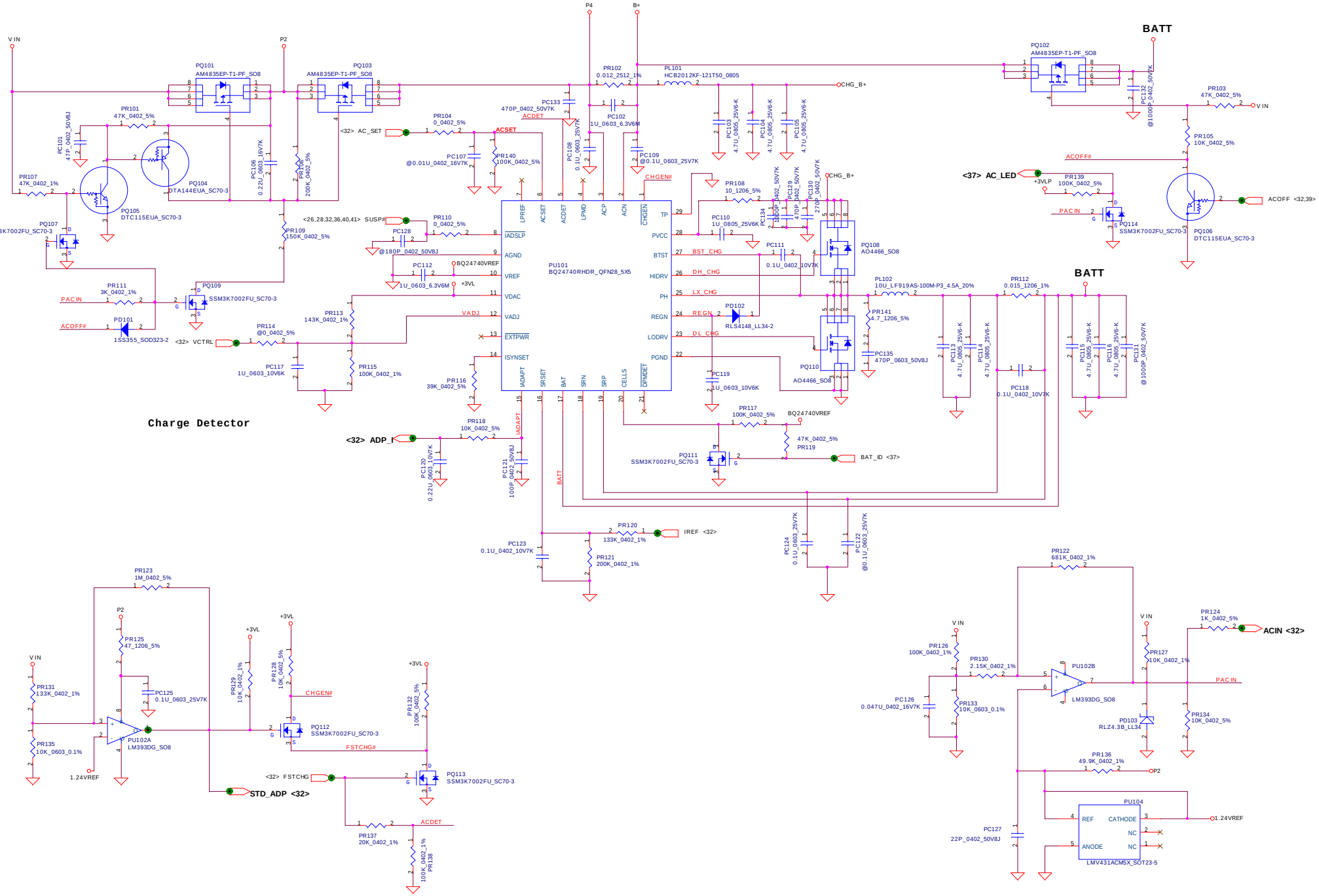
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **DC Connector/CPU_OTP**

Size	Document Number	Rev
	Montevina Blade UMA LA4101P	0.3

Date: Saturday, January 05, 2008 | Sheet 37 of 46



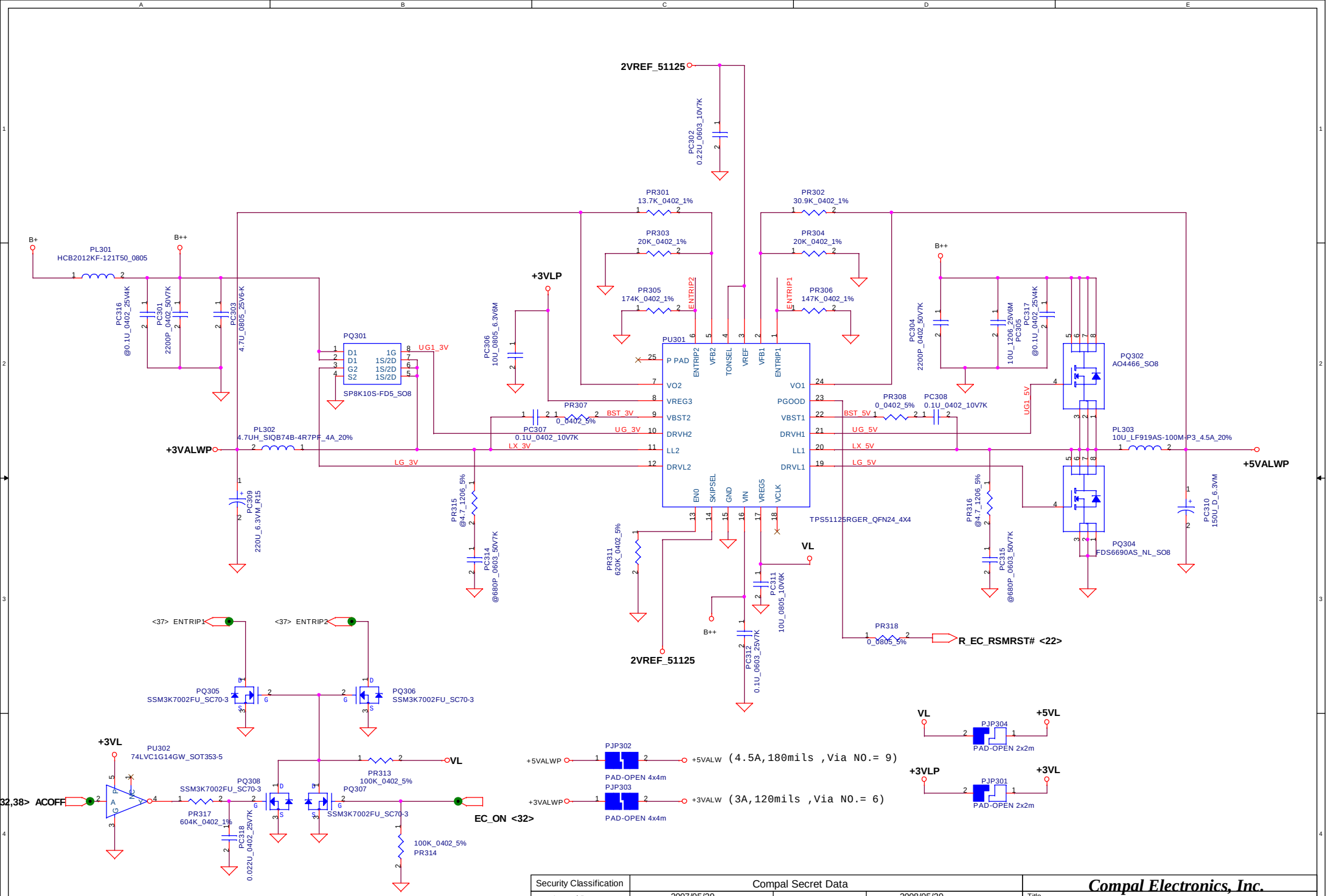
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **Charger**

Size | Document Number: **Montevina Blade UMA LA4101P** | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 38 of 46



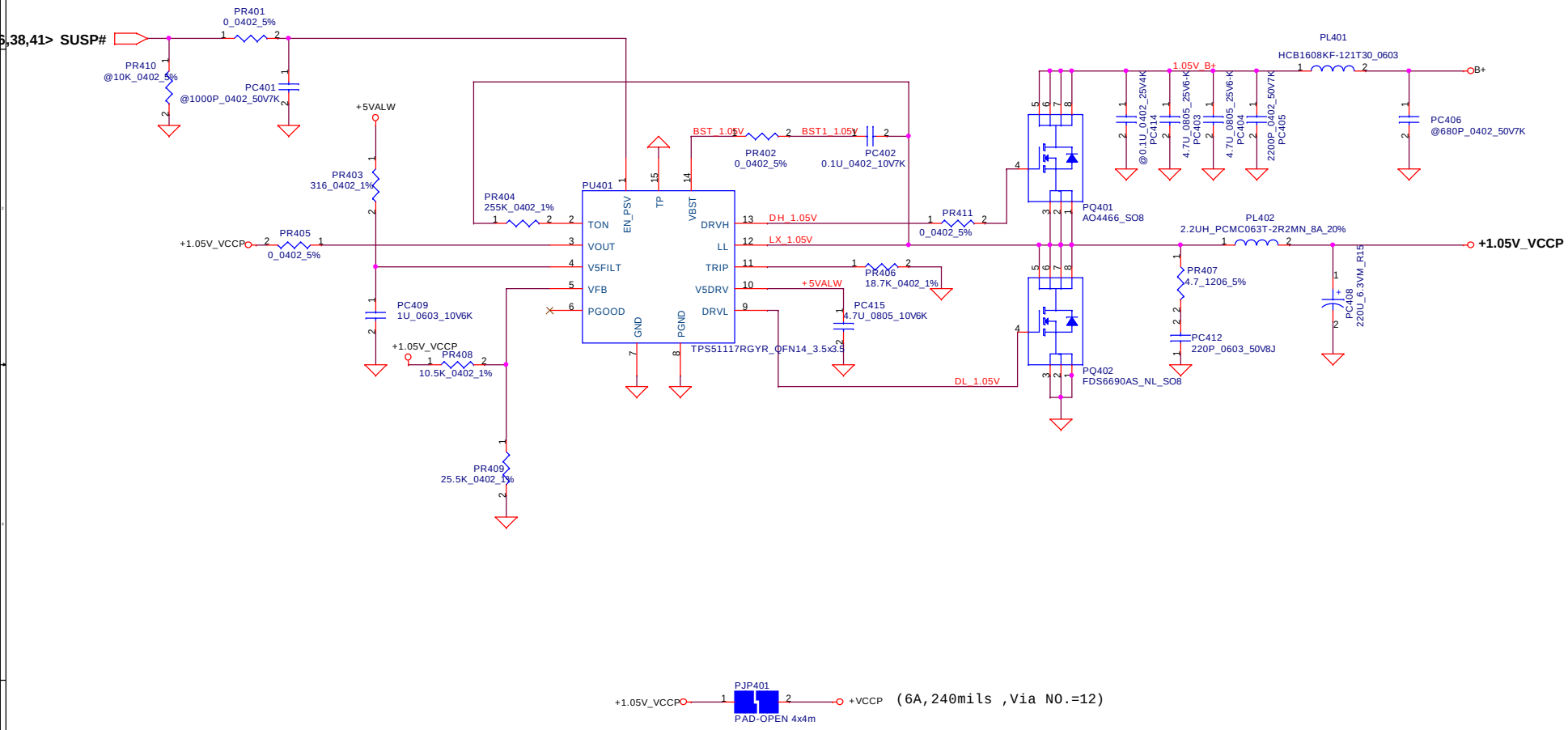
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **3.3VALWP/5VALWP**

Size	Document Number	Rev
	Montevina Blade UMA LA4101P	0.3

Date: Saturday, January 05, 2008 Sheet 39 of 46



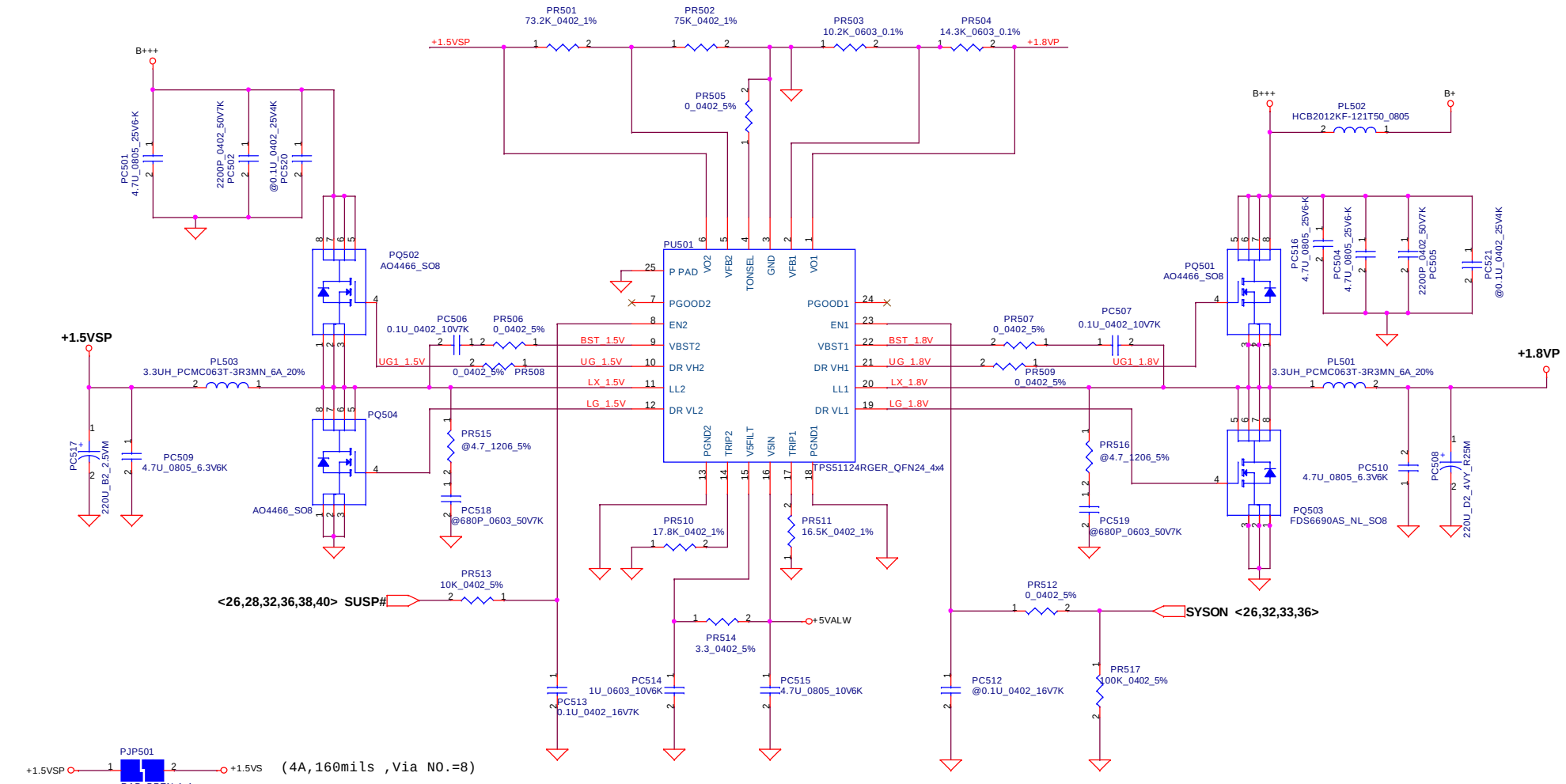
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **1.05V_VCCP**

Size | Document Number: **Montevina Blade UMA LA4101P** | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 40 of 46



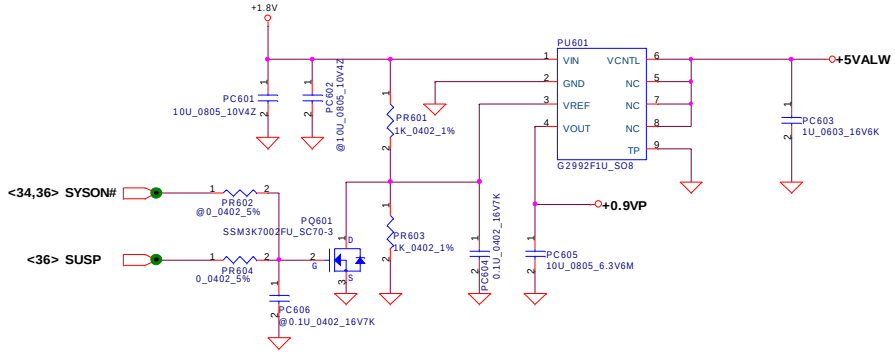
Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **1.5VSP/1.8VP**

Size	Document Number	Rev
	Montevina Blade UMA LA4101P	0.3

Date: Saturday, January 05, 2008 Sheet 41 of 46



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Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

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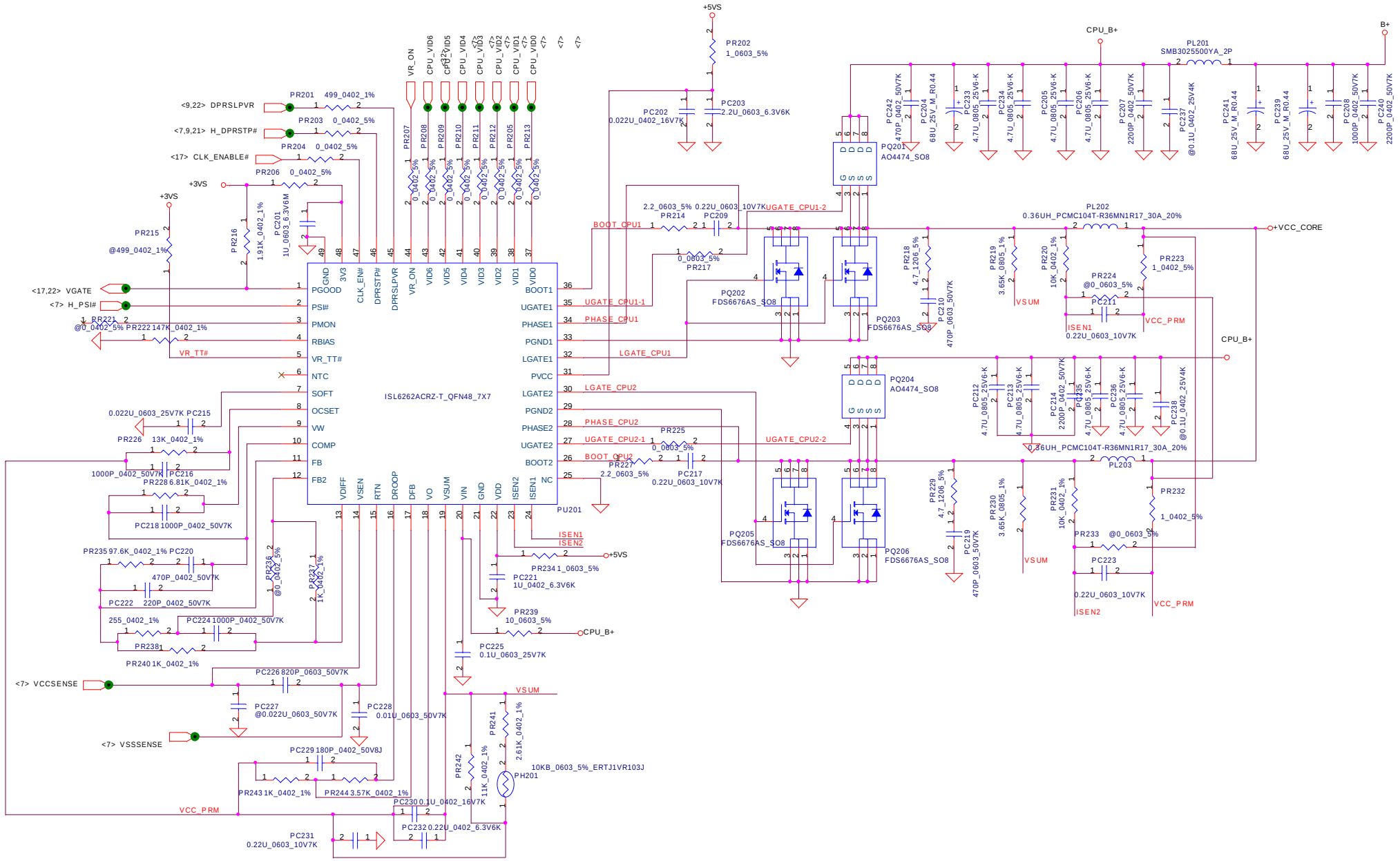
Title: **0.9VP/1.1V_PCIE**

Size | Document Number: **Montevina Blade UMA LA4101P** | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 42 of 46



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Title: **+CPU_CORE**

Size	Document Number	Rev
Custom		0.3

Date: Saturday, January 05, 2008 | Sheet 43 of 46

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Transation Fail	08	C41、C42、C43、C44 Change ESR=7m ohm	11/21	SI-1
2	Disable TV out function from Docking	11、34	R61、R62、R63 change to 75 Ohm、TV_DCONSEL_0、TV_DCONSEL_1 connect to GND	11/07	SI-1
3	Update Connetor Library		CRT(JCRT1)、HDMI(JHDMI1)、ESATA(JP53)、Finger print(JJP24)、FAN(JP2)、Speaker(JP60)、Multi bay(JP12)、Dual LED(D53、D12)	11/17	SI-1
4	Delete LVDS B channel	11、19	Schematic Delete	11/17	SI-1
5	USB camera Footprint error	19	Change U42 to G916-390T1UF SOT23, it adjustable mode, R1091=215K，R1093=100K	11/07	SI-1
6	Reserve Card reader D3E function	22、27	GPIO6= CR_CPPE#，GPIO22=CR_WAKE#	11/17	SI-1
7	Swap PCIE LAN and New card	22	Swap PCIE4 and PICE6	11/17	SI-1
8	Add HDCP ROM for ICH9M	22、31	Add HDCP ROM for ICH9M	11/17	SI-1
9	Change G sensor control from SB、LED drive by +5VS	22、33	Change G sensor control from SB	11/17	SI-1
10	Avoid Battery mode can't boot issue	22、39	Add +3VALW GD to EC_RSMRST# to fix Battery mode can't boot issue	11/17	SI-1
11	Add G sensor ST and Bosch	24	Add G sensor ST and Bosch	11/17	SI-1
12	Change LAN solution (Marvell to Realtek)	25	Change LAN solution (Marvell to Realtek)	11/17	SI-1
13	LAN can't work	25	U46 Change to correct transformer type	11/17	SI-1
14	Cardreader schematic review and update, add D3E function	27	R709-->10K、R402-->8.2K、R704-->Stuff、R705-->@、U37-->@、Cardreader LED-->+5VS、add D3E function	11/17	SI-1
15	Jack can't detect normal	28	R1059 change from 39.2 to 39.2K	11/17	SI-1
16	Speaker work un normal	28	Add and Stuff C1362、R1065、R596	11/17	SI-1
17	HP audio team recommend	28、29	C285~C292、C1352、C1354 change to 0.022U、Amp output setup to 15.6 dB、Reserve C305、C306 for GNDA and GND	11/17	SI-1
18	Audio jack can't detect normal	29	Add Pull up resistor R401 to +3VALW	11/17	SI-1
19	Docking HP audio test fail	29	Add C295□BC296 to avoid DC level, and add R409、R410 to reduce HP out level	11/17	SI-1
20	Leakage problem	32	Correct direction pretect leakage	11/07	SI-1
21	EC pin define update	32	Delete EC_PME#、SYSON PU、SUSP# PU、LID_SW# change to +3VALW、Delete CLKRUN#、R582->@ for C0 chip、CIR PU+5VL、add 100P to BATT_OVP(EC_recommend)	11/07	SI-1
22	Can't Hibernation(SLP_S4#)	32	Connect SLP_S4# to SB	11/17	SI-1
23	EC can't receive docking present	34	CONA# change +3VL	11/12	SI-1
24	HDMI can't detect	35	DDC _EN must enable 、TMDS_B_HPD# inverse	11/07	SI-1
25	LVDS power on timing	19	C238 change to 0.047u to meet TI timing	01/03	SI-2
26	Prevent WWAN nosie	21	Add 12p on HDA_SDOUT and HDA_SDOUT	01/03	SI-2
27	Power leakage	21、31	Change HDCP ROM to +3VS power plane	01/03	SI-2
28	Prevent WLAN leakage	26	Add Diode prevent WLAN leakage	01/03	SI-2

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Title: PIR

Size | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 44 of 46

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
29	New card PTH connector GND	26	New card PTH connector GND	01/03	SI-2
30	Change Cardreader LED control	27	Change Cardreader LED control	01/03	SI-2
31	Change SPDIF to SPDIF1	28	Change to SPDIF1	01/03	SI-2
32	Shut down pop noise	29	Change C293 to 1U	01/03	SI-2
33	Change BT power to +3VS	30	Change BT power to +3VS	01/03	SI-2
34	EMI Request	31	SPI_FSEL#、SPI_CLK_R、SPI_FWR# reserver RC	01/03	SI-2
35	Reserver 0 ohm co lay with common choke	35	Reserver 0 ohm co lay with common choke	01/03	SI-2
36	Sparate+5VS and +3VS power timing	36	Sparate+5VS and +3VS power timing	01/03	SI-2
37	Keyboard backlight reserve a 0805 size resistor	33	Keyboard backlight reserve a 0805 size resistor	01/03	SI-2
38	Change Lid switch connector type	33	Change Lid switch connector type	01/03	SI-2
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Title: PIR 2

Size | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 45 of 46

Version Change List (P. I. R. List) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	DC Connector /CPU_OTP	11/06	Compal	Add PD4 & PC12	Add PD4 & PC12	
2	39	3.3VALWP/5VALWP	11/06	Compal	for Layout	Change PQ301 cancel PQ303	
3	38	Charger	11/06	Compal	EMI solution	Add pc128	
4	43	+CPU_CORE	11/06	Compal	EMI solution	Add PC240	
5	39	3.3VALWP/5VALWP	11/14	Compal	for Layout	Change PL303 and PC310	
6	38	Charger	12/31	Compal	EMI solution	Add PC129, PC130, PC131, PC132, PC133	
7	43	+CPU_CORE	12/31	Compal	EMI solution	Add PC242	
8	39	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF	
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11							
12							
13							
14							

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Title: Power Changed-List History-1

Size: Custom | Document Number: Montevina Blade UMA LA4101P | Rev: 0.3

Date: Saturday, January 05, 2008 | Sheet 46 of 46